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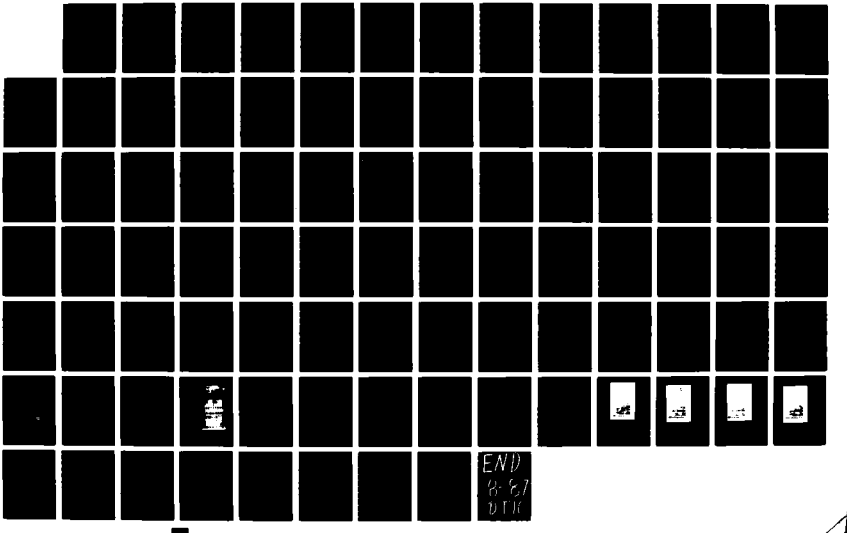

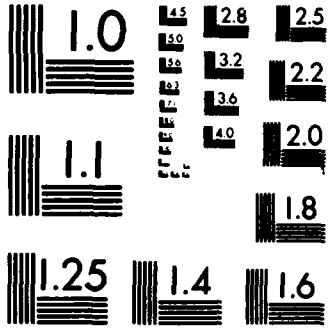


# BOARD LEVEL DEVELOPMENT OF THE AFIT VME DESIGN BOARD

THESIS

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Flight Lieutenant, PAKISTAN AIR FORCE

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THESIS

Presented to the Faculty of the School of Engineering

of the Air Force Institute of Technology

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Mohammad Siddique Javed, B.E.

Flight Lieutenant, PAKISTAN AIR FORCE

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Mohammad Siddique Javed

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## Abstract

This thesis investigates the design of an AFIT VME design board. This effort concentrated on implementing a prototype general purpose printed circuit board for SUN/3 Workstation. This thesis presents detailed design of the functional blocks like VME interface, testing electronics, and input/output interface. The board size is 14.5" X 15.125" and about half of the board is left unused for user application. The user can implement application specific circuitry in the provided space for testing in a real time environments.

An eight layer printed circuit board has been laid out and routed using DASH-PCB design system. The final product will be a valuable tool for testing VLSI chips and other applications in a real time environments.

# BOARD LEVEL DEVELOPMENT OF THE AFIT VME DESIGN BOARD

## I. INTRODUCTION

### 1.1. Background

The complexity and processing load in the latest applications of artificial intelligence and data management regularly exceed the speed requirements of typical Random Access Memories (RAM). The use of Content Addressable Memories (CAM) and Winograd Fourier Transform Algorithm (WFTA) chips are being considered at AFIT to greatly reduce the processing time in these applications. An extensive amount of research has been done at AFIT to create fast CAM and WFTA chips ( 10 ). As a part of this research, a CAM controller chip has been recently designed to control the operation of the CAM chips ( 4 ). There is also the need to design, implement, and fabricate a general purpose Printed Circuit Board (PCB) to implement specific application circuitry at a system level. For the Content Addressable Memory system this consists of the CAM chips, the CAM controller, and interface circuitry to test the CAM chips in real environments.

The use of a general purpose interface PCB for the SUN VME backplane will assist these and future research projects at AFIT. The VME bus has a master/slave asynchronous 32-bit data transfer format which supports multiple bus masters (processors and controllers), memories, and peripherals of varying speeds concurrently without slowing the bus to the slowest system device (14 : 69). The required interface hardware will be designed and put on the PCB so that all commonly used bus features are supported. Then AFIT VLSI chip research projects can be tested in a real or simulated environment on the board. Operation in a real time

environment allows testing and evaluation of all the chip operational parameters.

### 1.2. Problem Statement

The requirement, at present, is to create a printed circuit board to test AFIT 32-bit CAM chips and a CAM controller chip. Beside supporting the testing of the AFIT CAM chips, the AFIT VME Design Board (AVDB) is also required to be a general purpose board so that a variety of other applications can be tested using the same board design (sometimes called a board frame) ( 5 ). To support general purpose applications, the AVDB is required to have the following facilities:

a. Circuitry to interface with VMEbus as used in the Sun Workstation.

b. Circuitry to support testing of a variety of on board applications.

c. Circuitry to interface with parallel and serial Input/Output (I/O) devices.

d. An application area to support user specific circuitry which interfaces to the circuitry identified in a-c above.

### 1.3. Scope

The printed circuit board will be designed, laid out, and tested as a part of the AFIT CAM system development.

### 1.4. Summary of Current Knowledge

The complexity, speed, and large amount of circuitry required on a single Printed Circuit Board (PCB) motivates the development of mul-

tilayer high-density boards. Computer Aided Design (CAD) software tools are designed to help in design of such PCB's. AFIT has two such tools which perform PCB layout with automatic wire routing. The PCB software tool (on SSC VAX 11/780) has not been used in designing a realistic PCB and hence part of this research involves realistic use of this tool. AFIT also has DASH-PCB design system installed on IBM PC-AT which can be used to design printed circuit boards.

### 1.5. Standards

The AVDB will be designed per the VMEbus specification ( 8 ). It will be fabricated using the MOS Implementation Service (MOSIS) ( 9 ). To achieve high speed data transfer, the asynchronous VMEbus is preferred over Multibus, Qbus, and S-100 bus because of the larger bus data ( non multiplexed 32-bit data and 31-bit address), more error signals, and presence of extendible modes for future expansion. The VMEbus operates using a 16 megahertz clock and can handle data transfer rates up to 40 megabytes per second (14 : 69,70). AFIT has recently procured and installed Sun Workstations which use the VME backplane. They each have several extra slots which can be used to insert a PC board. Each slot has three sockets of 96 pins each and can hold PC board of size 15.8125" x 14.5". This is contrast to the VME specification where the double height Eurocard board is of size 6.299" X 9.187".

The size of the SUN VME board does not correspond to the double height VME standard board so as to increase the usable area and to achieve the extra space for the third 96-pin connecter used for extra power. The third connecter defined by SUN provides additional 25 Vdd, 25 Gnd, 6 VEE, 4 +12V, and 4 -12V pins. The SUN VME board has usable area 14"

X 15.25" which allows 427 IC equivalent per board at 0.5 square inch per IC. The SUN VME board provides usable area 3.68 times that of the standard VME double height board (16).

### 1.6. Approach

The general approach will be to first determine the requirements to be fulfilled by the AVDB. The necessary circuitry will then be designed to implement each requirement. CAD software tools will then be used for placement of the components at appropriate places on AVDB, and for automatically routing the interconnecting wires. Finally, the output file will be converted to a MOSIS-compatible file to get the board manufactured. Following design implementation of the printed circuit board, in a follow-on effort the CAM system will be constructed on the board and tested at AFIT using CAM project as the first application.

The design of the interface circuitry on the board must meet the requirements efficiently and at as low a cost as possible. Typical parameters like propagation delay and power consumption must be kept in mind to achieve the required product. Further a general purpose board will be created with 0.1 x 0.1 inch grid drilled holes in the application area to support wire wrap prototyping of further applications.

Computer Aided Design (CAD) software tools are available at AFIT for designing multilayer PCB's with automatic routing facility ( 5 ). Prior to the research reported here, the tools have not been used in actually designing printed circuit boards at AFIT. The existing PCB layout software can support board layouts with up to eight layers although currently the automatic routing facility works only for four layers. The other available tool is DASH-PCB design system which supports 10 layer

board designs. The number of available signal layers determines the allowable chip density on the printed circuit board. The eight layer board with four signal layers and four power/ground layers can increase circuit density by more than 100 percent as compared with four layer board with two signal layers and two power/ground layers( 6 ).

### 1.7. Organization of the Report

The remainder of this thesis contains six chapters. Chapter 2 describes the requirements definition and justification. Chapter 3 and 4 contain the system design and detail design respectively. Chapter 5 describes the results with necessary analysis. Finally Chapter 6 presents conclusions and recommendations for follow-on-work.

## II. SYSTEM REQUIREMENTS

The AFIT VME Design Board (AVDB) is a general purpose prototype board which is designed to fulfill certain requirements. These requirements are based in part on different possible applications of the board.

### 2.1. Statement of Requirements

The requirements to be fulfilled by the AVDB are categorized into following five different categories:

a. VMEbus interface

b. Testing electronics

c. I/O interface

d. User application area

e. Computer-aided design aids

### 2.2. VMEbus Interface

Since the AVDB is to be installed in a SUN Workstation, it should implement all the major VMEbus interface functions. The asynchronous VMEbus supports 32 bits of data and 31 bits of address on independent bus lines. The data and address lines coming into the AVDB should be electrically buffered to the VME data and address lines. The AVDB is required to have a selectable and maskable 31-bit address comparator to generate a board select control signal for each application such that the application may reside at a specific address or over a range of contiguous addresses. The AVDB should also provide seven independent priority interrupt lines. Direct Memory Access (DMA) to the VMEbus is also sup-

ported and requires use of other VME data transfer control lines.

### 2.3. Testing Electronics

The AVDB should hold commonly-used testing electronics circuitry such as a sequential memory address generator, storage register, clock generator, and address and data bus controller.

### 2.4. I/O Interface Electronics

The AVDB is required to have two parallel and two serial I/O ports to support communications between the application and external devices. The I/O interface electronic circuitry is required to be programmable from the user application area. Should these I/O ports be required to be accessed from the VME system, the additional interface required may be incorporated in the user application area.

### 2.5. User Application Area

The maximum possible area is to be provided on the AVDB where a specific application can be laid out and tested. All external interfaces (VMEbus, test control, external I/O) shall be supported by the AVDB.

### 2.6. Computer Aided Design Tools

It is required that the AVDB be designed using printed circuit board layout tools available at AFIT. The PCB software tool produces a CIF file compatible with MOSIS fabrication guidelines ( 9 ). Another PCB design tool, DASH-PCB, which will also be used in this research.

## 2.7. Justification of Requirements

The justification for all above mentioned requirements is discussed in the following paragraphs.

**VMEbus Interface Electronics.** The VME bus specifications as used by SUN are to be met because the AVDB once fabricated, will be used in a SUN/3 Workstation. To increase the available power and the usable area, the SUN/3 uses the triple height board which is not one of the VME standard boards (16). Functionally, the VMEbus can be summarized as having a master/slave asynchronous, nonmultiplexed data transfer structure, seven levels of priority interrupt, fault detection and control, and special transfer cycles ( 8 ).

In order to avoid any interference with other PC boards, data bits and address bits must be isolated, i.e. the AVDB should have its own address space. The AVDB monitors a specific address for a command from the host. When the VME host asserts this address, the 31-bit magnitude comparator signals the application electronics for further action (such as reset, data transfer, etc.). For interrupt- driven operation, the AVDB monitors the VMEbus interrupt acknowledgement signal (IACKIN*) coming in through the daisy-chain mechanism. On receipt of an acknowledgement signal from the VME host, the application interrupt request is acknowledged (if the user priority level matches the acknowledged level).

Apart from existing single byte data transfer capability, the user should be provided with a Direct Memory Access (DMA) facility to transfer data back and forth with the VME host. To be useful, the DMA

controller should support the fastest data transfer rate possible. The DMA controller is required to be programmable so that if it is provided the starting address and number of bytes to be transferred it transfers data automatically by generating further addresses. Data transfer is terminated after transferring the required number of bytes of data.

**Testing Electronics.** The AVDB should provide general purpose test circuitry for the application. Typical examples are address generator, storage/diagnostic register, and clock generator. Address generator is used to generate sequential addresses starting from some desired address. The storage/diagnostic register can either be used to store input/output data from the application or for some other diagnostic purposes. The register is directly connected to the board data bus. Transfer of data to or from the register is controlled by the application. The control signals to control and operate testing circuitry are terminated at the outer edges of the user application area.

**I/O Interface Electronics.** The AVDB contains up to two parallel I/O ports operating up to 1 megabytes per second and up to two RS232 serial I/O ports to facilitate communication with external devices when required by the application. All the ports have specific address, and each one can be addressed by the application when required. These direct ribbon cable I/O ports will be supported by programmable interface circuitry so that the application can perform any mode of operation when communicating with these devices.

**User Application Area.** As shown in Figure II-1, the user application area of the AVDB is left blank for the user to lay out an application

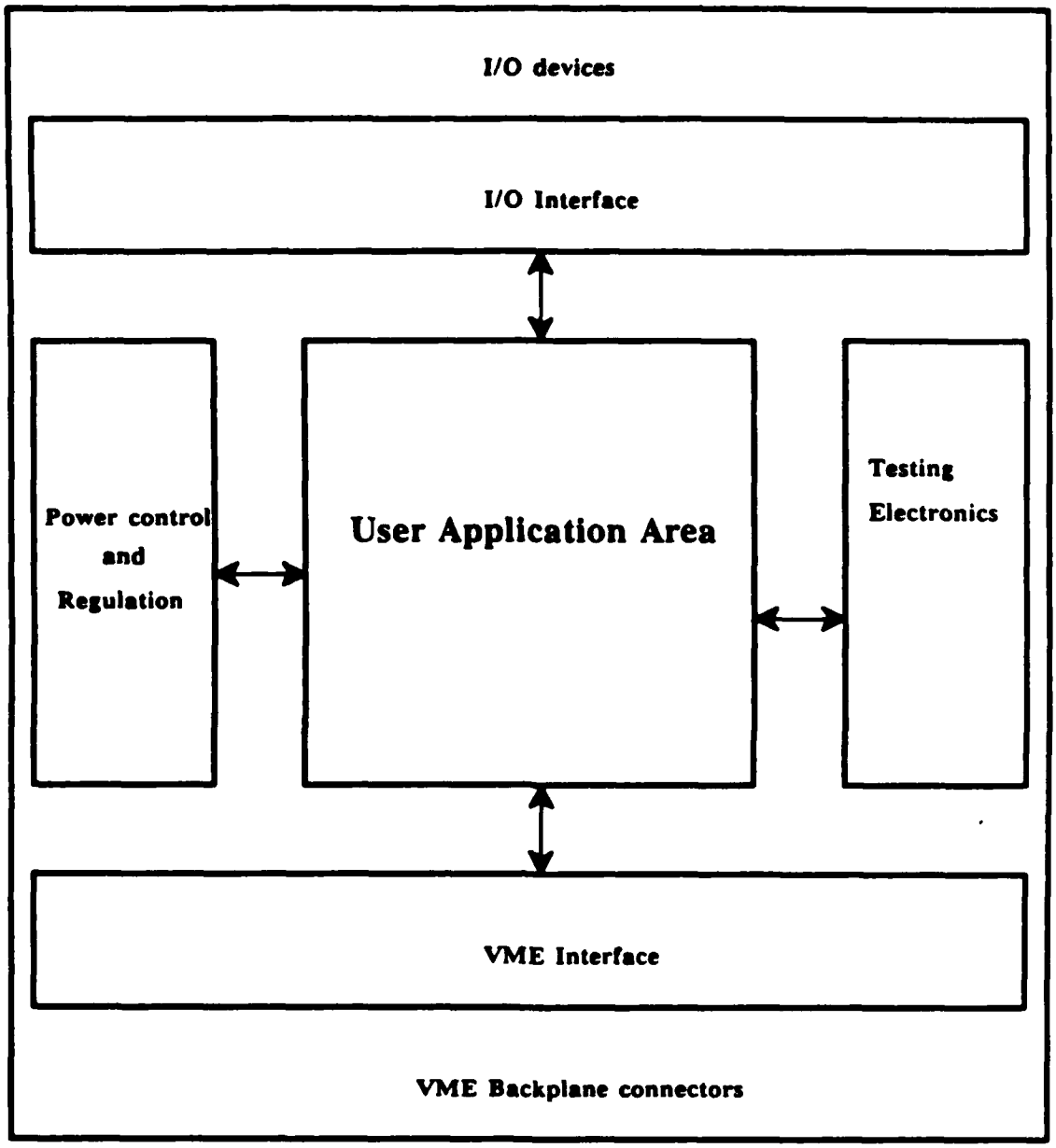


**Figure II-1. Major functional blocks of AVDB.**

circuit for testing. This provision is designed to hold application electronics including custom integrated chips. A ground and power routing grid is provided in this area. The general interface and testing electronics is compacted to the maximum extent to maximize the board area devoted to the user application. The data bits, address bits, control signals, system clock, power failure signal, and the rest of the required VME bus lines end at the edges of the user application area.

The design of a general purpose VME board will support a variety of applications and this eliminates the amount of effort required to design the bus interface and other commonly used circuitry. The board frame will be made available after testing, evaluation, and optimization. The database of this frame can be updated for a specific application. This allows user to concentrate in a particular research area for improvements because the rest of the onboard circuitry is already tested and isolated.

**Computer Aided Design Tools.** The fabrication requirements of MOSIS must be met to get the AVDB manufactured through MOSIS. For PCB layout software tool, the packages will be manually placed and then routing of the interconnecting traces will be done automatically using the batch mode of PCB router which supports 4 layer PCB designs.

In addition to PCB layout software, the Futurenet schematic designer (DASH-4) will be used to draw the AVDB schematic diagram. The pin processor will then be used to obtain a pinlist file. The pinlist describes the used pins of all onboard components along with their number and associated field. The DASH PCB router will be finally used to route the interconnecting wires on the specified layers of the board. The router accepts a

pinlist as an input file and also provides editing facilities to include the description of chip packages and placement of all the components. The DASH PCB router supports up to 10 layers board design which is an advantage over the PCB layout software for a congested board like AVDB.

# III. SYSTEM DESIGN

The system design of the AFIT VME Design Board (AVDB) is described in this chapter. The system design described achieves a solution for the problem statement within the specifications of Chapter II.

The problem statement restated is: to design, implement, and fabricate an AVDB to hold user applications such as the CAM project which consists of CAM chips, a controller chip, and other circuitry. The AVDB is to be fabricated by MOSIS. The general specifications are given in chapter II.

The system design is covered in two levels in this chapter. These levels are the top level and the first level design. The lower levels of the design are given in the next chapter (Detailed Design). The first level design is a decomposition of the top level.

## 3.1. Top Level Design

The top level overview of the AVDB is drawn in Figure III-1. The VME interface portion of the AVDB consists of the interface electronics required which interfaces the VME host with the users application. The VME system 31-bit data and address busses are isolated from the board data and address busses using tri-state transceivers. A manually-selectable 32-bit address magnitude comparator (to be described later) is incorporated to establish the address space of the user application. A seven-level interrupt mechanism including daisy chain operation is also incorporated to service the user application as necessary. A DMA controller is also included to provide high-speed data transfer with the VME

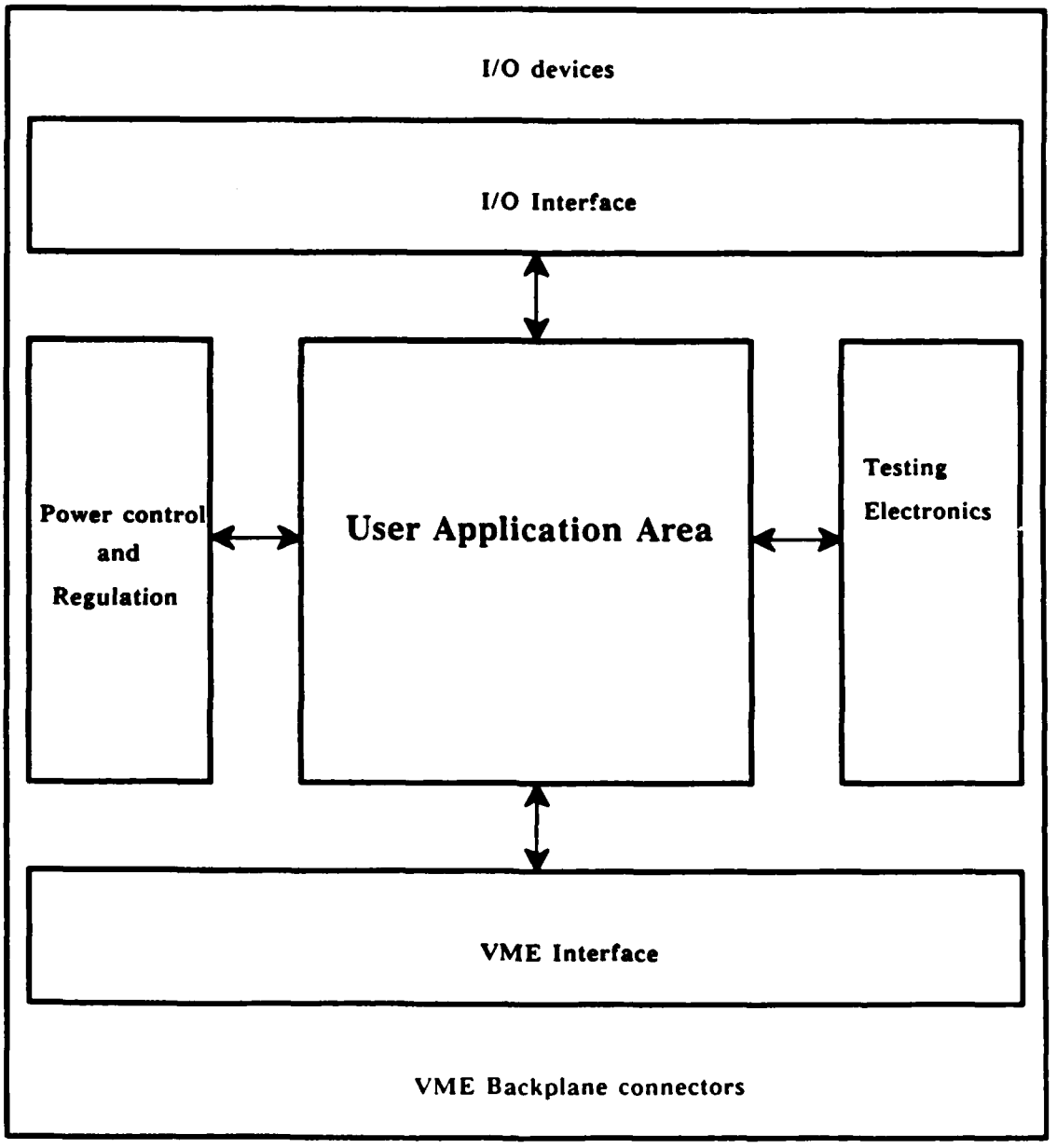


**Figure III–1. AVDB top level system activity diagram.**

host.

The testing electronics portion of the AVDB contains some of the general purpose testing circuitry which may be useful for the user application. The testing circuitry includes a 31-bit address generator, a storage/diagnostic register, a bus controller, and a clock generator.

The I/O interface electronics meets the requirements of communication between external devices connected to on-board parallel or serial ports. The AVDB supports two parallel I/O ports and two serial I/O ports. Separate connectors are provided for each port at the outer edge of the AVDB. The interface circuitry includes the port address decoding.

If the user application requires more power control and/or regulation than that provided by the interface, components for this purpose can be located in the power control and regulation area of the board. The most commonly used supplies (+5 volts, +12 volts, and ground) are provided to the user application area by the VME bus interface.

### 3.2. First Level Design

We now look at the next lower level of system definition. This more detailed presentation of the design addresses the VME interface, testing electronics, and I/O interface.

### 3.3. VME Interface Electronics

The functional blocks of VME interface electronic circuitry are shown in Figure III-2. They are:

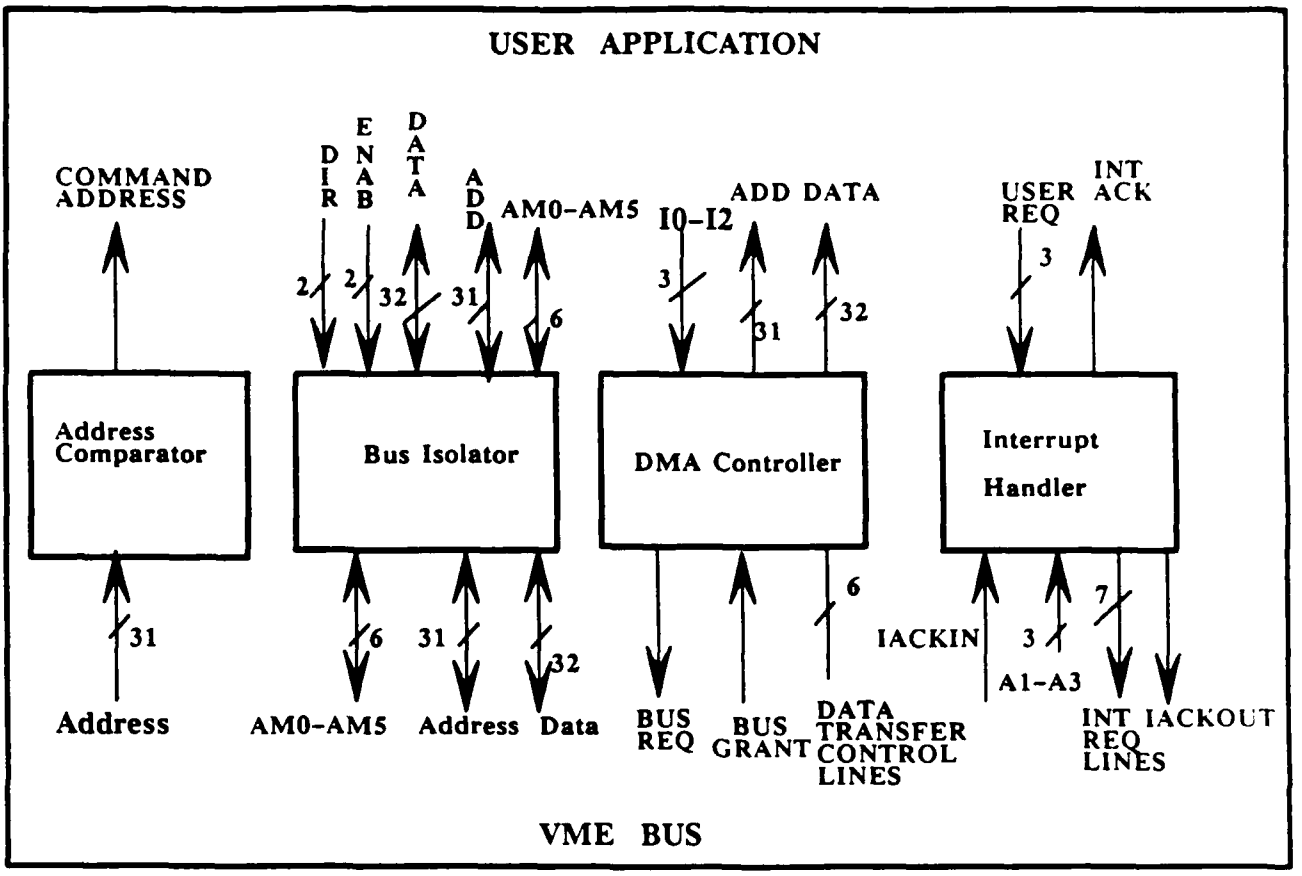


**Figure III-2. Functional blocks of VME interface electronics.**

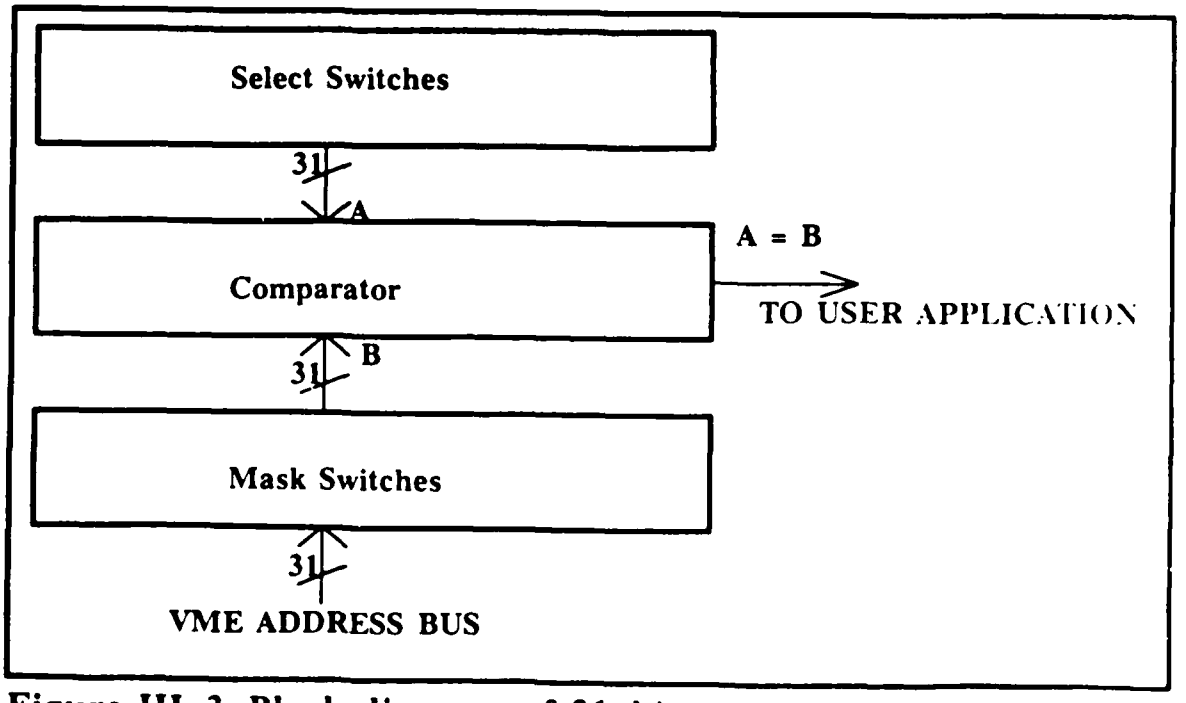


**Figure III-3. Block diagram of 31-bit magnitude comparator.**

**Address Comparator.** The selectable 31-bit address magnitude comparator is connected to the 31 address bits of the VME bus. The block diagram of the address comparator is shown in Figure III-3. The 32-bit select address is manually set using binary DIP switches (Select Switches). The comparator asserts address select bit (A = B) when the VME bus address is equal to the manually selected address. The incoming VME bus address bits can be masked as required by setting masking DIP switches (Mask Switches). This implements a regional contiguous address space or a specific address select. Apart from the conventional design, laser programmable address comparators will be included in a VLSI VME interface chip which has been designed and is being implemented. The address modifier signals (AM0-AM5) will also be checked by VIC chip for their validity.

**Bus Isolator.** Tristate bus transceivers are used to isolate the VME data and address busses. Control bits are set by the user to connect or disconnect the busses when required by the user application. It is important that these isolators have minimum propagation time and set time and meet the VME specifications. The timing specifications are further discussed in Chapter IV.

**DMA Controller.** The DMA controller provides high-speed data access to VME host memory. It is connected to address and data busses through tristate buffers. The DMA controller can be programmed by the user application. Such programmable commands consist of the starting address, number of bytes to be transferred in case of block transfer. The six address modifier bits of the VME bus will be set for either single byte

(8-bit), or double byte (16-bit), or quad byte (32-bit) data transfer as required by the application. The VME bus supports DMA transfer rates up to 40 megabytes per second. The DMA controller will be included in VME interface chip as an ultimate solution.

**Interrupt Handler.** The interrupt handler transfers asynchronous request from the user application to the VME host interrupt request lines and replies via acknowledgement on receipt of IACKIN* signal from the VME bus. A daisy chain operation is also performed by the interrupt handler. The block diagram of the interrupt handler is drawn in Figure III-4.

The user application sets three request bits (001 through 111) depending upon the desired priority (001 is the lowest priority). The user request bits are decoded and the appropriate VME interrupt request line is set LOW. The VME bus interrupt handler then acknowledges the interrupt by setting IACKIN* signal LOW and the priority of acknowledged request is set on the three Least Significant Bits (LSB) of the address bus (A1-A3). The IACKIN* signal is routed through the system boards in a daisy chain fashion ( 8 ). On receipt of the IACKIN* signal the AVDB interrupt handler compares the three LS address bits with three bits user encoded request. The user request acknowledge (URACK) signal is set HIGH if both inputs to the comparator are equal. If they are not equal, the Interrupt Acknowledgement Out (IACKOUT*) signal is set LOW for daisy chain operation. The VME interface chip will handle the interrupt mechanism and hence the above mentioned conventional design will be included in the chip.

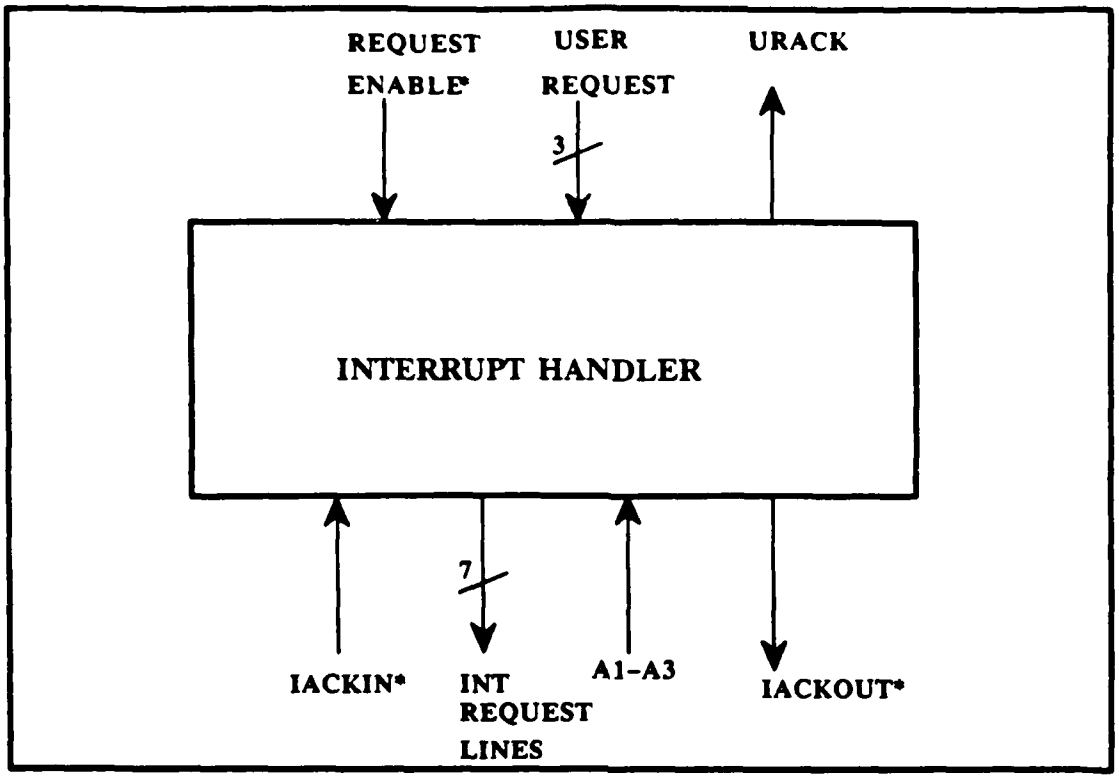


**Figure III-4. Block diagram of interrupt handler.**

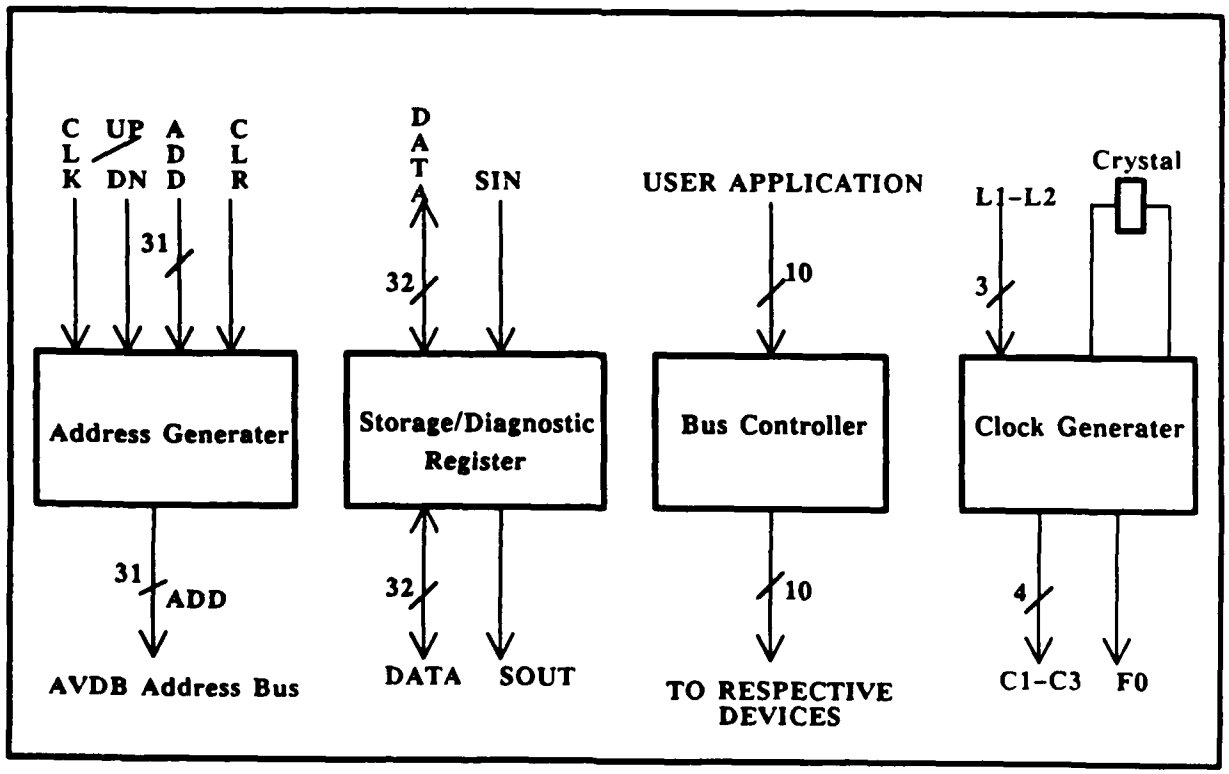


**Figure III-5. Functional blocks of testing electronics circuitry.**

### 3.4. Testing Electronics

The functional blocks of testing electronic circuitry are shown in Figure III-5.

**Address Generator.** The 31-bit address generator receives initial input from the user application. The up or down count mode can be selected by setting the appropriate mode of operation. It is a 31-bit binary counter with output connected to the board address bus. The address generator can operate on up to 6 megahertz clock. By setting the appropriate mode of operation starting address can be loaded in or the contents can be cleared. The address generator is connected to the board address bus through tristate buffers so that it remains completely isolated when not in use.

**Data Storage.** The data storage block of the AVDB contains a 32-bit data register. It is a bi-directional parallel input/parallel output and serial input/serial output register. It provides a 32-bit parallel data path between the user application and the board address bus. It also contains a 32-bit shadow register for performing serial shadow register diagnostics and/or writable control store loading (further explained in chapter IV) [ 2 : 8-13]. It can be used to pin-point digital system hardware failures in a systematic and well-understood fashion. The detailed circuit design of the storage register is discussed in chapter IV.

**Bus Controller.** The bus controller controls the data and address busses and helps enabling only the required tristate buffers between busses and the devices they are connected to. It is an ten bit high-speed parallel register, each bit being used to control one device. The device

which needs to be connected receives the enabling bit and the remaining devices are disabled. The specific use of each bit is explained in chapter IV.

**Clock Generator.** It is a general purpose crystal controlled clock generator. It has microprogrammable clock cycle length to provide significant speed-up over fixed clock cycle approaches ( 2 : 5-220). The clock generator can run at frequencies up to 20 megahertz. One of the eight cycle lengths can be generated under microprogram control using the cycle length inputs L1, L2, and L3. All the control inputs and the clock outputs are provided to the user application. A two phase clock can be either obtained by using a separate IC package or by using the output waveforms of the same clock generator along with other necessary circuitry. The detailed design of the clock generator is discussed in chapter IV.

### 3.5. Input/Output Interface

The functional blocks of serial and parallel I/O interface circuitry are shown in Figure III-6. There are two parallel and two serial I/O ports to communicate with external devices. Each serial channel is RS232 compatible and each parallel port is eight bit wide with additional signals available for control and synchronization.

**Parallel I/O Interface.** This electronic circuitry interfaces the AVDB with two 8-bit bidirectional I/O ports (A,B). The interface circuitry is programmable, and the control and data information is passed on the eight least significant bits of the data bus. The control signals and data are separated by setting the C/D control signal.

**Serial I/O Interface.** Serial I/O provides interface circuitry for two full duplex serial I/O devices on two different channels. The interface

supports data transfer on eight least significant bits of data bus and the transfer rate can be as high as 550 kilobytes per second in synchronous mode. The circuitry is programmable and is RS232 compatible.

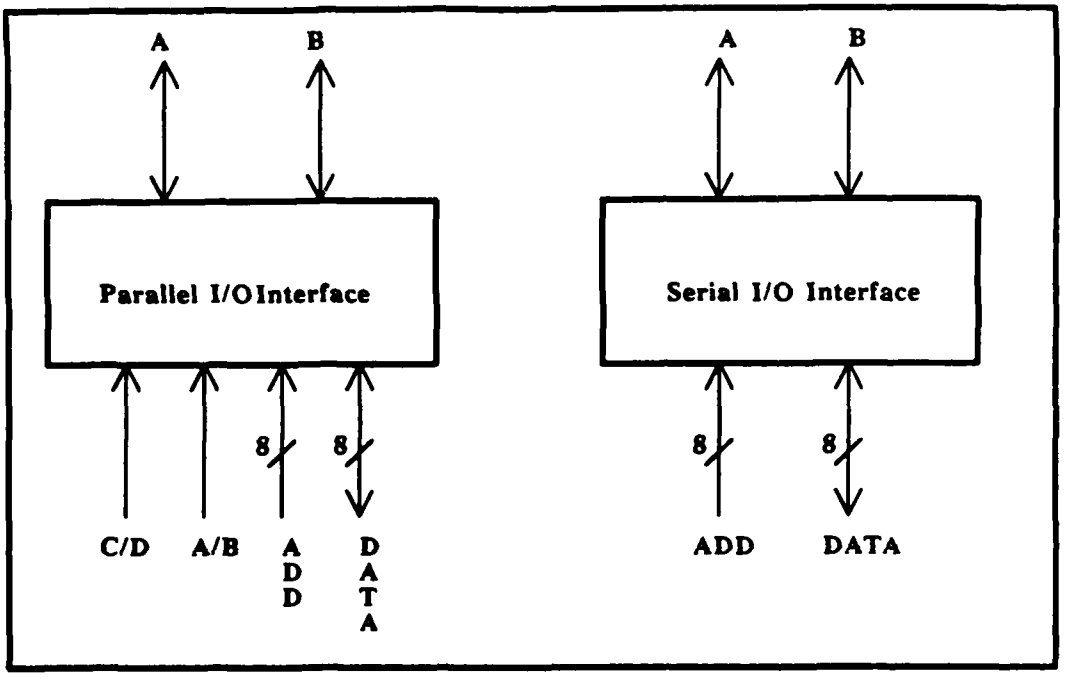


**Figure III-6. Functional blocks of I/O interface circuitry.**

### 3.6. AVDB Layout

The overall layout of the AVDB is shown in Figure III-7. The data and address busses are routed on three sides of the AVDB and are connected to the different blocks as required. The lower portion of the AVDB plugs into the VME backplane, and the upper edge contains sockets for serial and parallel ports as described earlier. The address comparator, DMA controller, and interrupt handler will be replaced by a single 84-pin VLSI VME Interface Chip (VIC) to economize the board space and

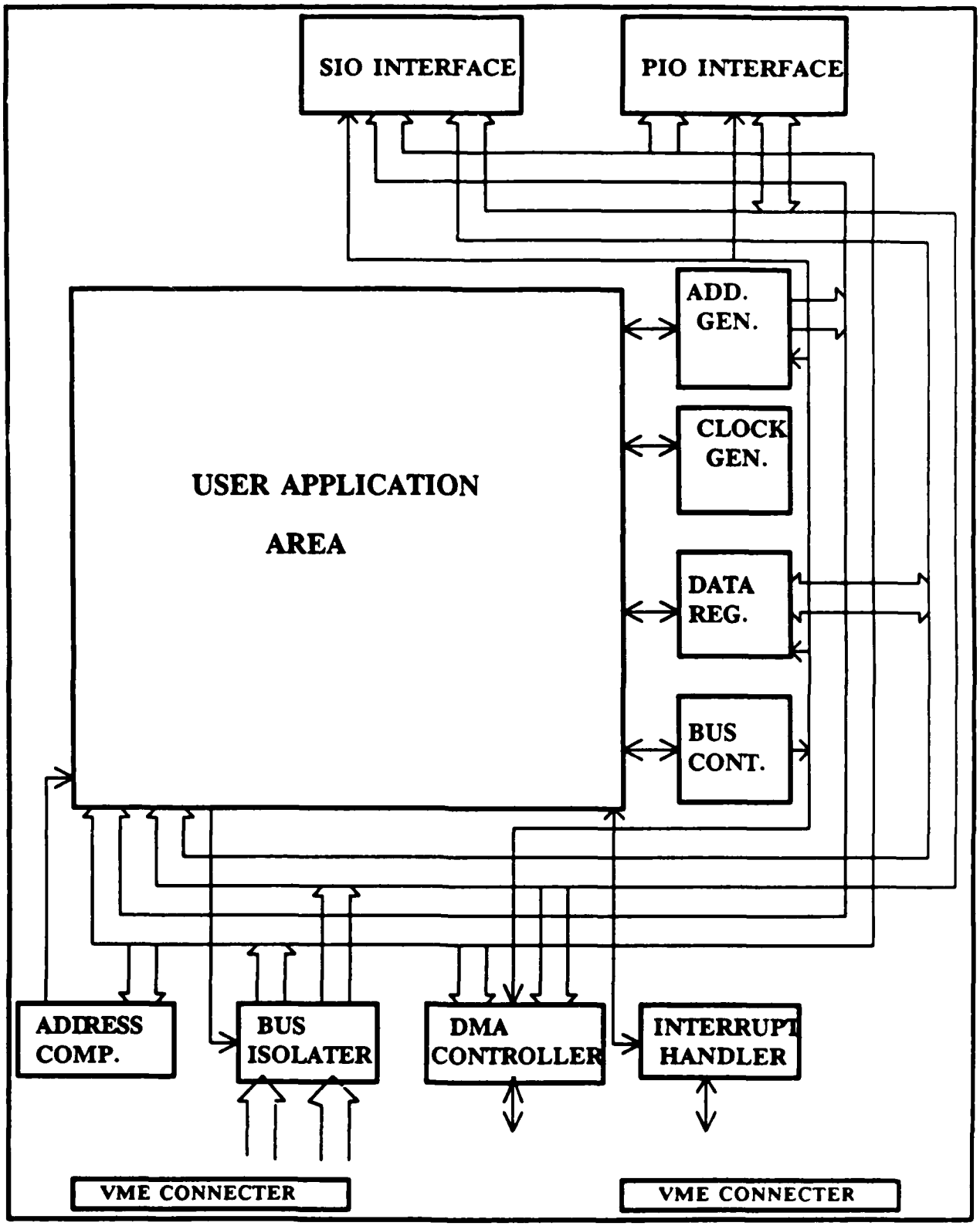


**Figure III-7. The overall AVDB layout of functional blocks.**

to achieve the greater efficiency.

The size of the AVDB is 15.8125" X 14.5". The user application area, which is about 7" X 7", is left blank for any specific application. All interface signals are terminated at outer edges of the user application area and sufficient power and ground points are also provided at different locations to reduce the wire lengths if wire wrapping is chosen for implementation of the user application.

# IV. DETAIL DESIGN

## 4.1. Overview

The first two design levels of the AFIT VME Design Board (AVDB) have been discussed in Chapter III. In the top level the functional blocks were shown and discussed. The first level of the design presented further detail of these functional blocks. The inputs and outputs of these blocks were described which showed how the system fulfills the requirements discussed in Chapter II. Chapter IV discusses the detailed implementation of the blocks. The schematic diagrams are drawn and explained in this chapter, and also the timing analysis and different applications of these blocks are discussed. Half of the AVDB is used by the VME interface circuitry, testing circuitry, and I/O interface circuitry. The remaining half of the board (7" x 7") is left blank for the user application .

In particular, The user application area is sufficiently large to mount and route interconnecting wires for 16 84-pin CAM chips, one 84-pin CAM controller chip, and other chips required by CAM system. The following paragraphs present the detail design of each block discussed in chapter III.

## 4.2. VME Interface

The VME interface consists of 31-bit magnitude comparator, DMA controller, and interrupt handler. These blocks were first designed using conventional integrated circuits but the amount of space consumed by these packages was not acceptable and also the propagation delay was not desirable. To overcome these shortcoming a VLSI 84-pin chip (VIC) has been designed and is being implemented (4). The VIC chip occupies only a 1.21 square inch space, whereas the packages of conventional design

consume about 15 square inches of board space. The conventional design is discussed in the following paragraphs and VIC chip will be briefly described lateron in this chapter.

### 4.3. 31-bit Address Comparator

The purpose of the 31-bit address comparator, as discussed earlier, is to constantly monitor for a specific address on the 31-bit VME address bus.

**Schematic Description.** A conventional, 31-bit magnitude comparator using existing and commercially available components is implemented by cascading four 8-bit identity comparators ( 74F521). The 'F521' is a high speed expandable 8-bit comparator which compares two words of up to eight bit each. It provides a LOW output when two words match bit by bit. The schematic diagram of the cascaded 31-bit comparator is drawn in Figure IV-1. The comparator is comprised of U1, U2, U3, and U4. As shown in the schematic the VME 31-bit address bus is connected to the four manually selectable 8-bit mask switches (U5 through U8) which are used to mask out the address bits as required. The bits which are to masked out are disconnected by setting the appropriate mask switches OFF, and the corresponding inputs to the magnitude comparator are set HIGH by pull-up resisters (U9 through U12). The desired address to be monitored is selected on four 8-bit select switches ( U13 through U16). LOW is set on these switches by setting them to the ON position and HIGH is set by setting them to the OFF position via the pull up resisters (U17 through U20). The outputs A = B of each comparator are connected to a five input NOR gate U21 (74S260). The NOR gate output is HIGH when all its inputs are low indicating the desired address on the VME address bus. The output of U21 is provided to the application.

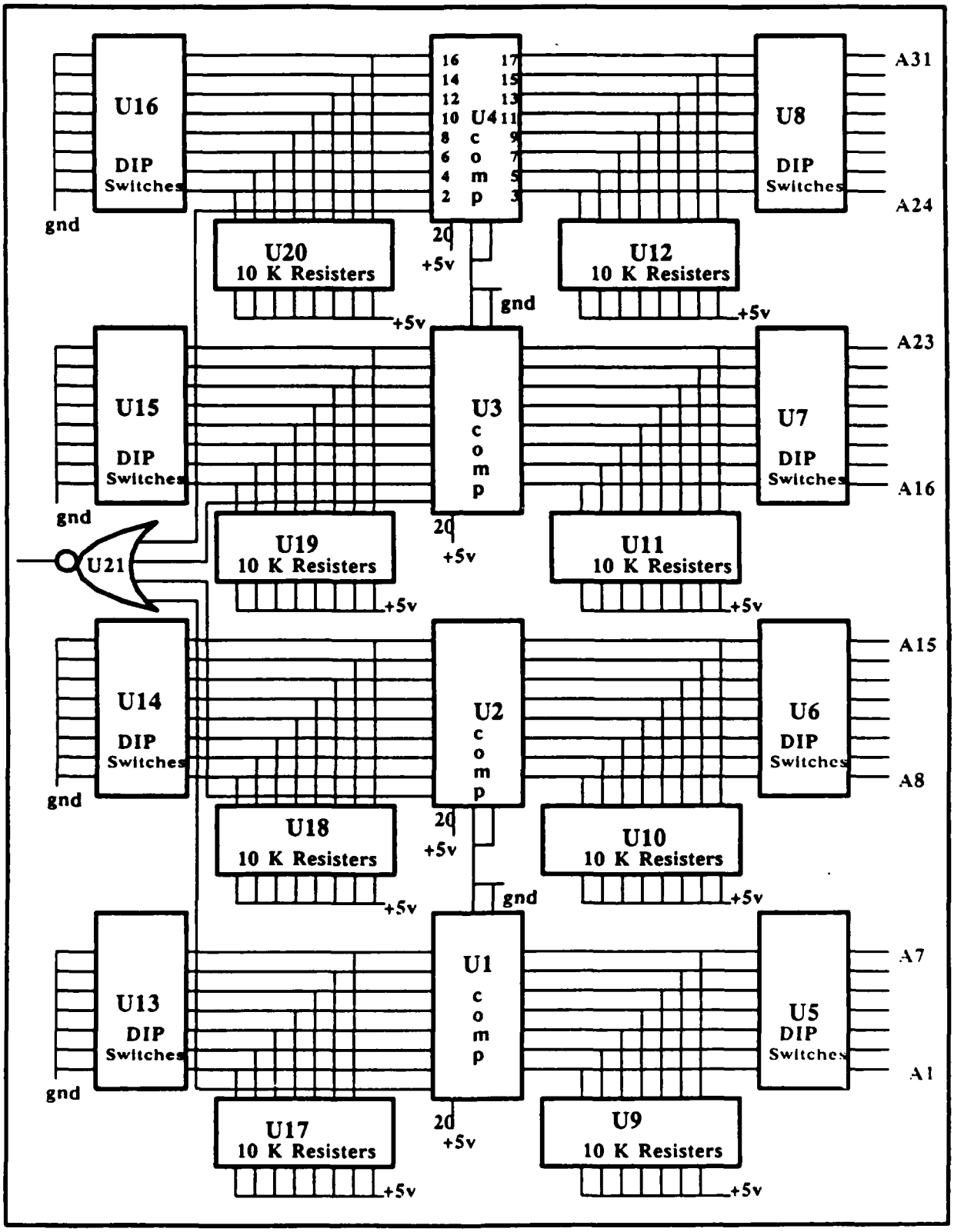


**Figure IV-1. Schematic diagram of address comparator.**

**Electrical Characteristics.** The typical power supply current required for a 'F521' is 21 mA (3 : 4-377). The maximum propagation delay of the comparator is 11 ns. The NOR gate draws maximum power supply current of 20 mA and the typical propagation delay is 6 ns. Hence the overall propagation delay of the address comparator is 17 ns which is one-third of the 20 M HZ clock cycle used in VME system. The user application should respond to this address in the next clock cycle.

**VIC Comparator.** The VIC chip will have four such laser programmable magnitude comparators. The extra comparators will provide additional address space. The VIC chip will also ensure the validity of the address modifier signals (AM0-AM5). Apart from reducing the propagation delay the VIC chip will eliminate the space being consumed by a number of packages used in the conventional design.

### 4.4. Bus Isolator

It is important to isolate the VME system data and address busses from the respective busses of the AVDB. The purpose is to allow the AVDB to access these busses when the host permits it to do so. It is responsibility of user application to connect or disconnect these isolators at an appropriate time i.e. the VME busses should be connected to AVDB busses on acknowledgement of the user bus request or interrupt from the host.

**Schematic Description.** Two separate isolators are implemented for data and address busses. These isolators are similar, and hence only one data bus isolator will be described. The 32-bit data bus isolation is achieved by using four '54LS245' octal bus transceivers. The schematic diagram of the isolator is drawn in Figure IV-2. The 'S245' are designed for

asynchronous two way communication between busses and are shown in the Figure as U22 through U25. The enable input (ENAB) from the user application controls the operation of the transceivers. If enable bit is HIGH, these transceivers are at high impedance i.e. disconnected. The isolator allows data transmission from system bus to the AVDB bus, depending upon the logic level at the direction control input (DIR) provided by the application. DIR = LOW allows data transmission from the system bus to the AVDB bus while DIR = HIGH directs data in the opposite direction (12 : 3-826).

**Electrical Characteristics.** The isolator has typical enable and disable times of 40 and 25 ns respectively, and the port-to-port propagation delay time is 8 ns. The electrical and switching characteristics are discussed in detail in TTL data book (12 : 3-828).

### 4.5. DMA Controller

The conventional design of DMA controller using commercially available components is discussed below. The AFIT VIC chip will meet the same functional specifications as minimal, but is not yet formally designed.

The DMA operation starts by requesting permission to use the VME data transfer bus. The request is made by pulling any one of the four VME bus request lines (BREQ0* through BREQ3*) LOW. The VME system provides an efficient allocation method for the data transfer bus. The bus request is acknowledged by the host, and is propagated through a daisy chain operation. After the bus request has been acknowledged, the data transfer is initiated by the DMA controller starting a read or write cycle. The VME bus has no restriction on the amount of time that the master (the DMA in this case) may keep control of the bus after another master

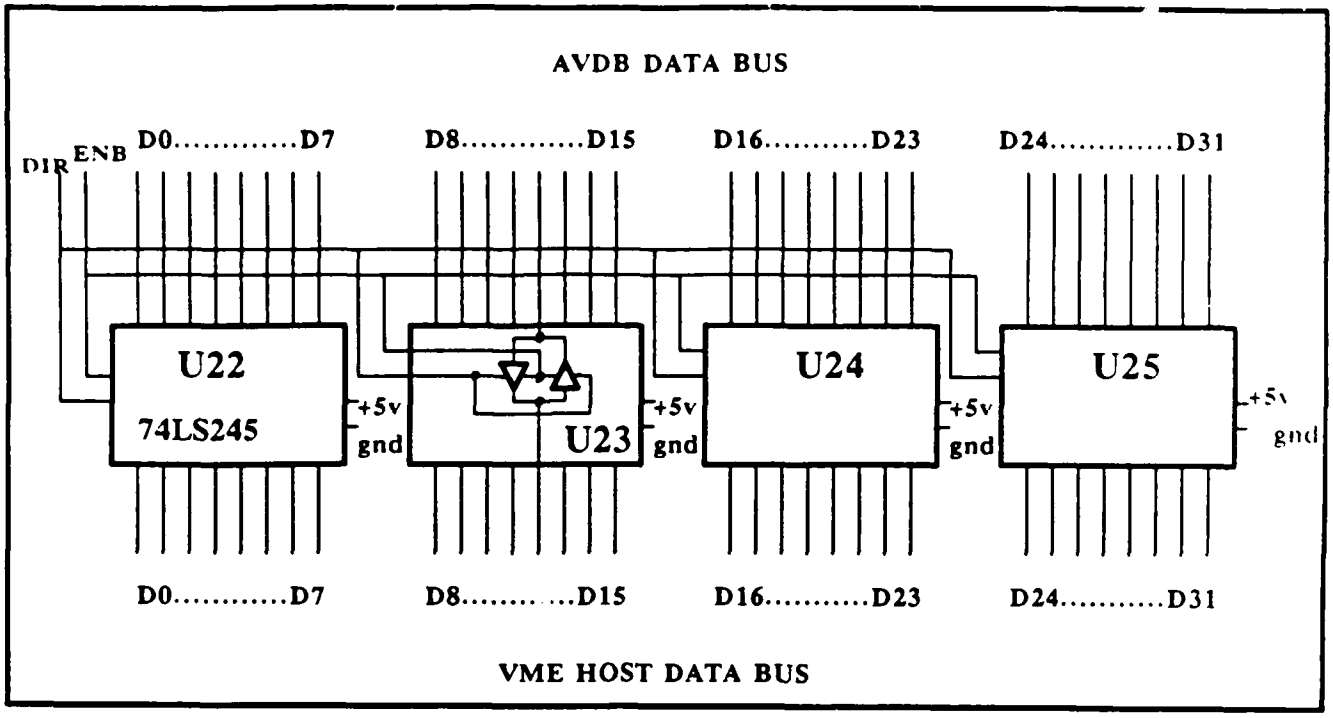


**Figure IV-2. Schematic diagram of data bus isolator.**

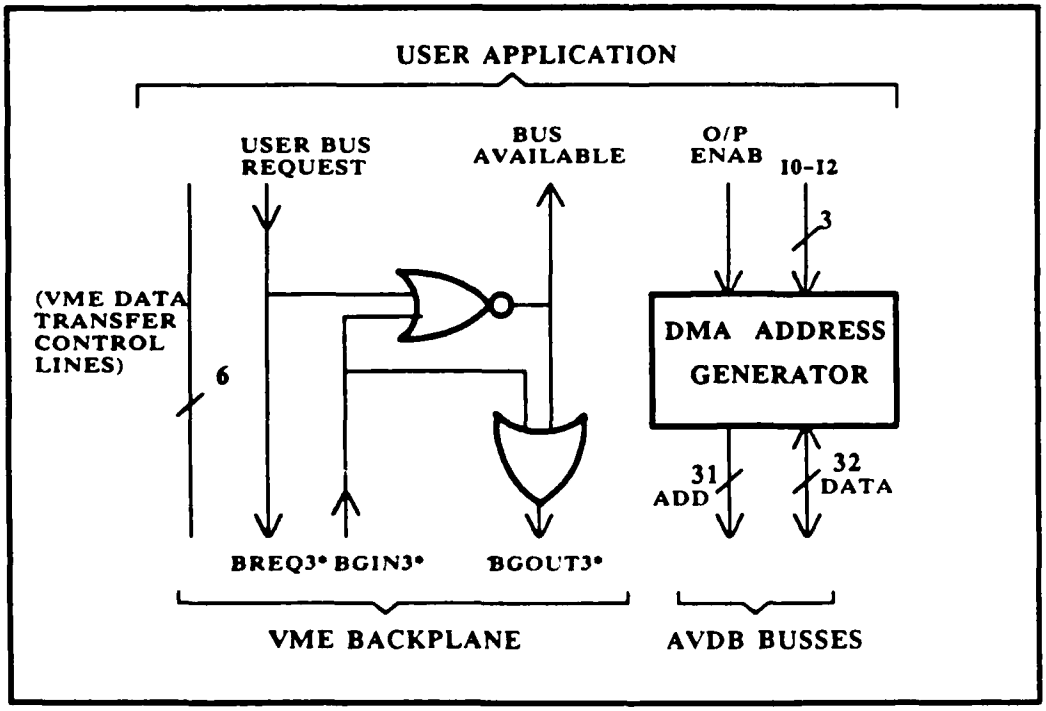


**Figure IV-3. Block diagram of DMA controller.**

has issued a bus request. However the SUN/3 will release the bus as soon as it completes the cycle that may be in progress when the bus request arrives (7 : 6). The SUN/3 uses only bus request level 3 and so bus grant in and out, BG3IN* and BG3OUT*, are only used by using single level arbitration. The address modifier lines (AM0 through AM5) are set by the user application according to the required data width being transferred (single, double, or four bytes).

If during DMA transfer the bus is taken away, the address generator will keep the word count and address to be started during the next available time. The bus request is raised again and this process continues until the desired number of bytes of data has been transferred. The overall block diagram of the DMA controller is drawn in Figure IV-3. The output of DMA address generator is enabled when the acknowledgement is received on BG3IN* line. The BG3OUT* is set LOW for daisy chaining if BG3IN* is received without the AVDB bus request.

**Data Transfer Control Lines.** While transferring data certain control lines must be driven during the read/write cycle at appropriate time. The AS* (Address Strobe) and DTACK* (Data Transfer Acknowledgement) lines must be driven for all transfers, whereas the other control line values are operation dependent. The AS* line is set LOW to inform all slave modules that the address in now stable on the address lines. The DS0* (Data Strobe), if set LOW, means that the addressed byte can be found on bus data lines D00 through D07, and DS1*, if set LOW, means that the addressed byte can be found on bus data line D08 through D15. The LWORD* (Long Word) line (LOW) specifies that 32-bit data will be transferred on data lines D00 through D31. The DTACK* line is driven by

the slave to indicate that the data was successfully transferred in a write cycle and also to indicate that the data has been received from memory and has been placed on on the data bus in a read cycle. The BERR* (Bus Error) line is driven by the slave to indicate that the data was not written during a write cycle or that it could not be retrieved in a read cycle. The AS* must be driven LOW when the rest of the master lines are valid. The slave must hold both DTACK* LOW and data valid as long as the data strobe is LOW.

**DMA Address Generator.** The programmable 32-bit DMA address generator is implemented by using four cascadable Am2940 8-bit DMA address generator chips. It generates the memory address, word count, and a DONE signal for DMA transfer operation. Its distinctive characteristics include the provision for four types of programmable control modes with memory address increment/decrement and the execution of eight different instructions.

**Functional Description.** As shown in Figure IV-4 the Am2940 address generator consists of an eight bit address counter, an eight bit word counter, transfer complete circuitry, a three bit control register, and an instruction decoder. The address counter, which provides memory address during DMA transfer mode, is an eight bit binary up/down counter with full lookahead carry generation. Under instruction control, the address counter can be enabled, disabled, and loaded from the data inputs D00 through D07. The address counter output can be enabled on to the tri-state address outputs A00-A07 under control of the output enable input DEA*. The word counter, which maintains and saves a word count, is similar in structure and operation to the address counter.

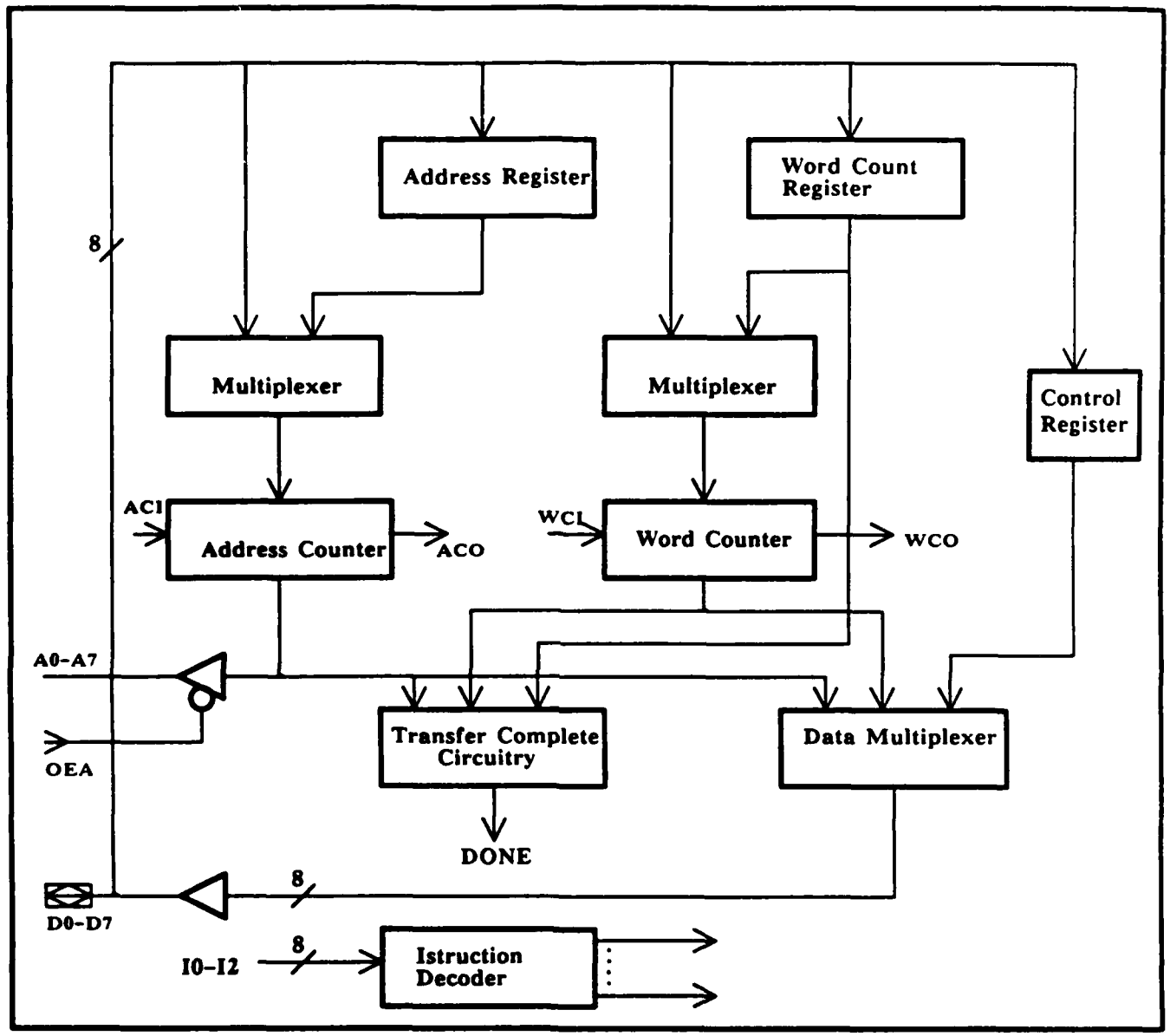


**Figure IV-4. Block diagram of Am2940 address generator.**

The transfer complete circuitry is a combinational logic network which directs the completion of the data transfer operation and generates the DONE output signal. The DONE signal is an open collector output, which can be dot-anded between chips. The instruction decoder generates the required internal control signals as a function of the instruction inputs I0-I2. The clock input is used to clock the address and word counter on low-to-high transition. Under instruction control the 3-bit control register can be loaded or read from the bidirectional data lines. The control register bit 0 and 1 determine the control mode and bit 2 determines whether the address counter increments or decrements.

**Control Modes.** The Am2940 address generator has four control modes and any one can be selected by setting bit 0 and bit 1 of the control register. In control mode 0 the word count is loaded in to the word counter and it is set to decrement on every clock pulse. The DONE signal is generated when the word counter reaches zero. In control mode 1 the word count is loaded in to the word count register and word counter is cleared. The word counter is then set to increment on every clock pulse. The DONE signal is generated when the word count output becomes equal to the word count register.

In control mode 2 the initial memory address is loaded in to the address counter and the final memory address is loaded in to the word counter. The word counter is disabled and the address counter decrements or increments (depending on the control register bit 2) on low-to-high transition of clock input. The transfer complete circuitry compares the address counter with the word counter and generates DONE signal during the last word transfer. In control mode 3 word counter is loaded with the two's

complement of the number of data words to be transferred. The word counter is set to increment and its carry output signal WCO* indicates that the last word is being transferred. The DONE signal is not required in this mode.

**Instruction Set.** The Am2940 instruction set consists of eight instructions which are described in Table IV-1. Any particular instruction can be executed by setting appropriate inputs I0-I2.

**Table IV-1. Am2940 instructions**

| I0 | I1 | I2 | Octal Code | Function | Mnemonic | Control Mode |
|---|---|---|---|---|---|---|
| L | L | L | 0 | Write Control Register | WRCR | 0,1,2,3 |
| L | L | H | 1 | Read Control Register | RDCR | 0,1,2,3 |
| L | H | L | 2 | Read Word Counter | RDWC | 0,1,2,3 |
| L | H | H | 3 | Read Address Counter | RDAC | 0,1,2,3 |
| H | L | L | 4 | Reinitialize Counters | REIN | 0,2,3 |
| H | L | H | 5 | Load Address | LDAD | 0,1,2,3 |
| H | H | L | 6 | Load Word Count | LDWC | 0,2,3 |
| H | H | H | 7 | Enable Counters | ENCT | 0,1,3 |

**Schematic Description.** The schematic diagram of the DMA address generator is drawn in Figure IV-5. The four Am2940 (U26 through U29) are cascaded to design 32-bit address generator. The tristate address outputs are directly connected to the AVDB address bus. However the

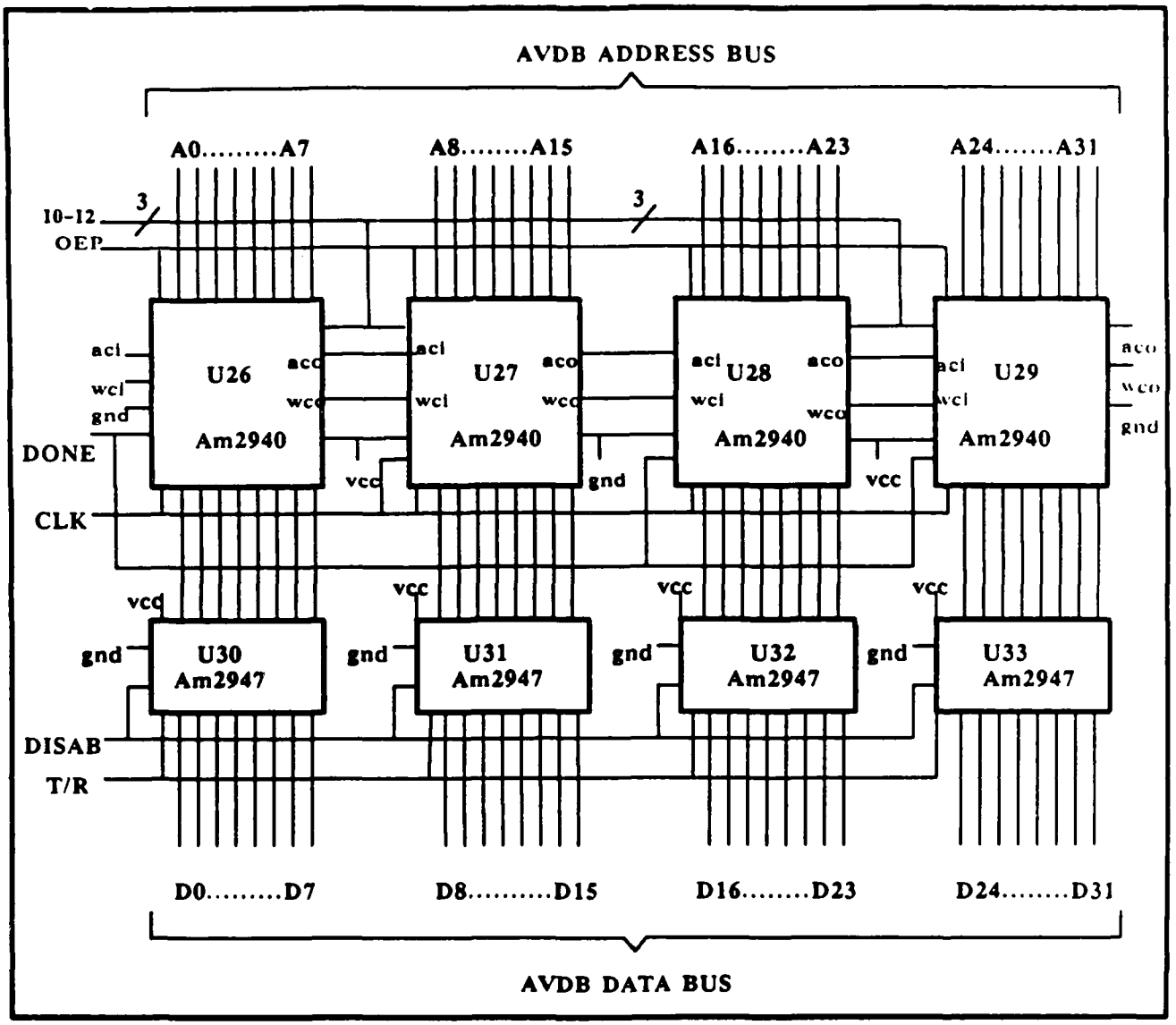


**Figure IV–5. Schematic diagram of DMA address generator.**

bidirectional data lines are connected via four Am2947 bus transceivers (U30 through U33). The DONE output from each address generator are anded (U34) to generate the effective DONE signal. The I0-I2 inputs select one of the eight instructions. The ACI* and ACO* are the carry-in and carry-out of the address counter respectively. The WCO* and WCI* are the carry-out and carry-in of the word counter register respectively. The CP input is the clock input and the internal registers and counters change their state on low-to-high transition. The OEA* signal, if set LOW, puts the address on the AVDB address lines.

**Switching Characteristics.** The setup times, relative to the low-to-high clock transition, are 27, 49, 34, and 34 ns for D0-D7, I0-I2, ACI*, and WCI* and their respective hold times are 6, 5, 5, and 5 ns. The maximum clock frequency is 16 M HZ with minimum LOW time of 23 ns and minimum HIGH time of 35 ns. The disable and enable time from I0-I2 to D0-D7 is 42 ns and from OEA* to A0-A7 is 30 ns.

### 4.6. Interrupt Handler

The AFIT VIC will have the interrupt handling block which will functionally work the same way as discussed below by using commercially available components. The inclusion of interrupt handler in VIC chip will eliminate the space consumed by conventional packages.

The AVDB interrupt handler receives a 3-bit encoded user interrupt request and then pulls down one of the seven VME interrupt request lines. The system interrupt handler acknowledges the request on IACKOUT* line which is propagated through the boards in daisy chain manner and the corresponding priority is put on the VME address lines A1-A3. The AVDB interrupt handler receives the acknowledgement and compares the user

application request with A1-A3. The user application is only responsed to if the raised priority interrupt was acknowledged. If some other interrupt is acknowledged then the IACKOUT* signal is set LOW for next board on system.

**Schematic Description.** The schematic diagram of the AVDB interrupt handler is drawn in Figure IV-6. The 3-bit user request is received in the 3 to 8 decoder (U35), which then pulls the appropriate VME bus interrupt request line. The decoder is implemented with SN74S138, 3 to 8 decoder. The user request lines UREQ0-UREQ2 are connected as three select input to the decoder. The enable input to the decoder is provided by the user application.

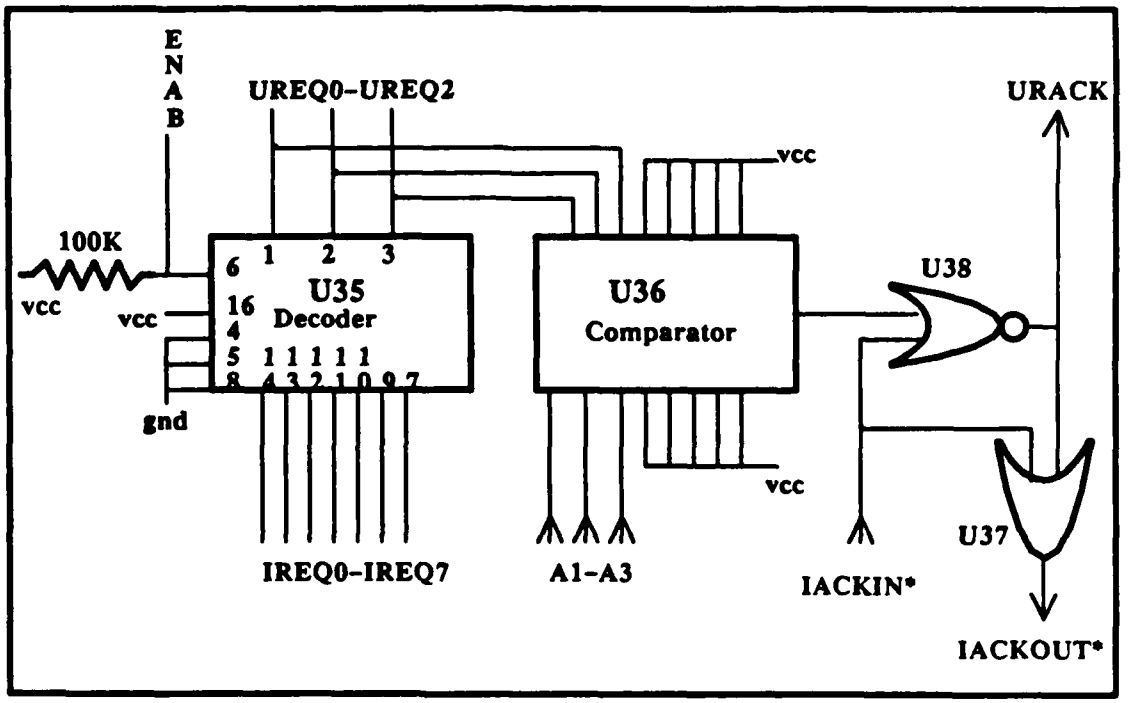


**Figure IV-6. The schematic diagram of the AVDB interrupt handler.**

The comparator U36 (SN74F52) is an eight bit magnitude comparator which compares two inputs, the user request and the acknowledged interrupt level from the VME system. The U38 (74S260) NOR gate gives acknowledgement to the user application if the comparator output is LOW (both inputs are equal) and the VME system IACKOUT* line is LOW. The user then places the status ID on data bus and drives DTACK* LOW to signal system interrupt handler. If the comparator output is HIGH and IACKIN* is LOW i.e. the interrupt acknowledgement is for some other board , the IACKOUT* signal is set LOW for the next board on the system.

**Electrical Characteristics.** The maximum propagation delay of the decoder is 11 ns after selecting the enable input. As the AVDB will not be used in the first slot of VME system, the magnitude comparator time 11 ns is not an effective delay for user application because the IACKIN* is propagated through the boards whereas acknowledged interrupt request level is put on A1-A3 lines. The IACKIN* signal is further delayed by U38 (74S260) NOR gate by 6 ns. For daisy chaining operation the IACKIN* is propagated through U37 (74S32) two input OR gate and is delayed by 13 ns.

### 4.7. Clock Generator

The clock generator provides a general purpose crystal controlled clock with microprogrammable clock cycle length. It is implemented by using Am2925 clock generator and microcycle length controller.

**General Description.** The Am2925 is a single-chip general purpose clock generator and generates four different simultaneous clock output waveforms. One-of-eight clock cycle lengths can be generated under

microprogram control using the cycle length inputs L1, L2, and L3. Crystal control oscillator is designed to run at frequencies from 0 to 40 M HZ. The control functions include Run, Halt, Single-step, Initialize, and Ready/Wait control. The description of the inputs and outputs is given in the following paragraphs.

**Inputs.** The L1, L2, and L3 are the clock cycle length control inputs and select one of the eight microcycle waveform patterns F3 through F10 as shown in Figure IV-7. The HALT* and RUN* control inputs will determine that the clock outputs are stopped and not stopped respectively. The First/Last input is a HALT* time control input which if HIGH, causes a Halt to occur when output C4 is LOW and C1, C2, and C3 are HIGH. The First/Last input if LOW, causes the Halt to occur when C4 is HIGH and C1, C2, and C3 are LOW. The SSNO and SSNC are the single step control inputs which allow system clock cycle single stepping while HALT* is LOW. The WAITREQ* input causes the clock outputs to Halt during the next oscillator cycle. The Cx input is the wait cycle control input and the control outputs respond to a wait request(WAITREQ*) one oscillator clock cycle after this goes LOW. The READY* input is used to continue normal clock output patterns after a wait state. The INIT* input is used for initialization during power up of the system.

**Outputs.** The C1, C2, C3, and C4 are the system clock outputs and their timing is determined by clock cycle length controls L1, L2, and L3. F0 is the buffered oscillator output and WAITACK* output indicates that all clock outputs are in "WAIT" state.

**Schematic Description.** The schematic diagram of the general purpose clock generator is drawn in Figure IV-8. All the inputs and outputs

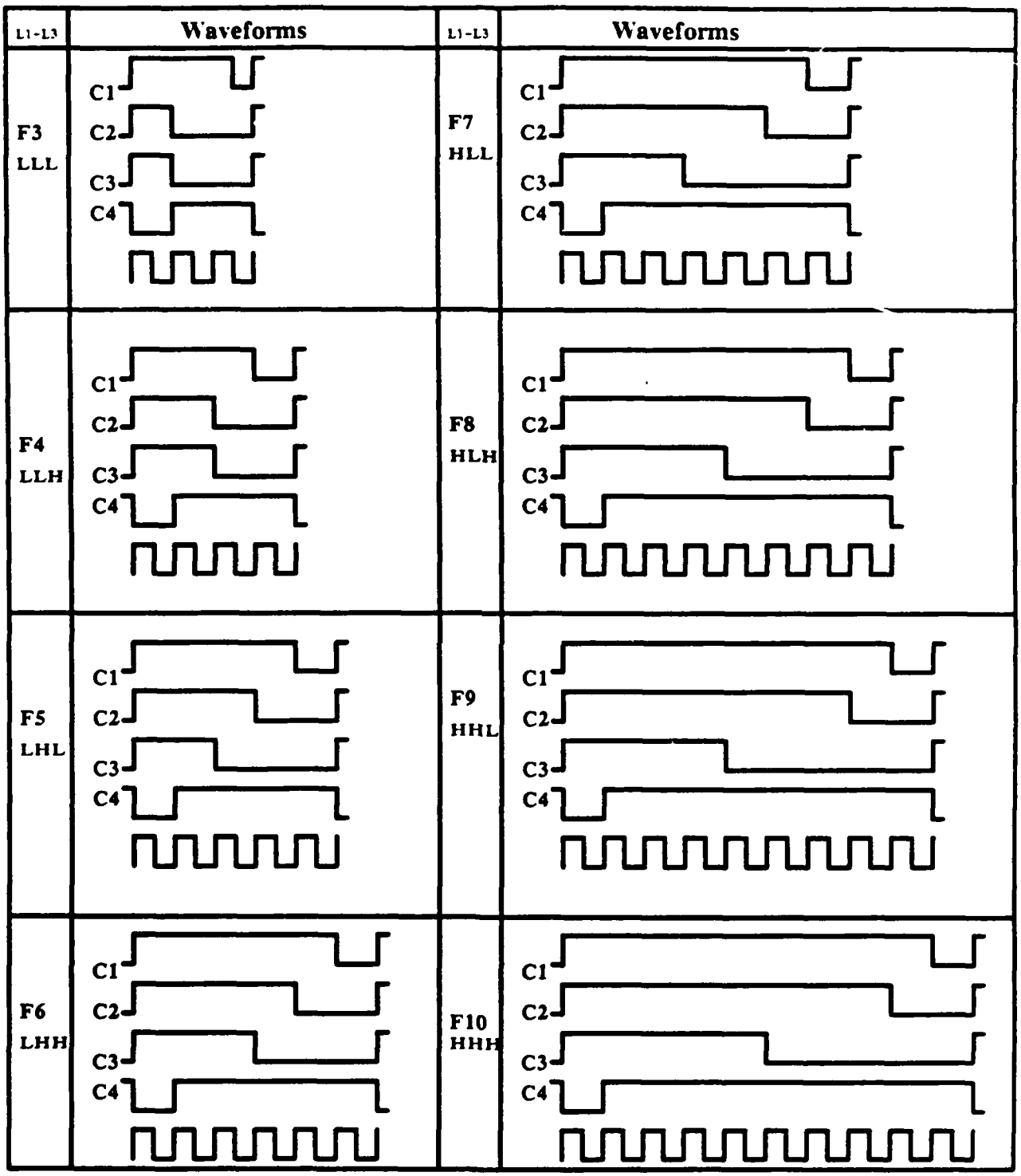


**Figure IV–7. The clock waveforms of clock generator.**

are connected to the application area. The oscillator is designed for 1-40 M HZ operation. The capacitor C1 and C2 are of 68 PF and are used to provide crystal loading. The resister R is not required for 6-40 M HZ crystals but below 6 M HZ the resister should be added to eliminate the third harmonics. Two points P1 and P2 are left open which can either be connected with a wire(for 0-6 MHz) or an appropriate resister R can be put across these points. The value of R should match the impedance of C2 and is calculated as:

$$R = 1 / ( 2 \pi f C)$$

Where f is the crystal frequency and C is the capacitance of the capacitor C2.

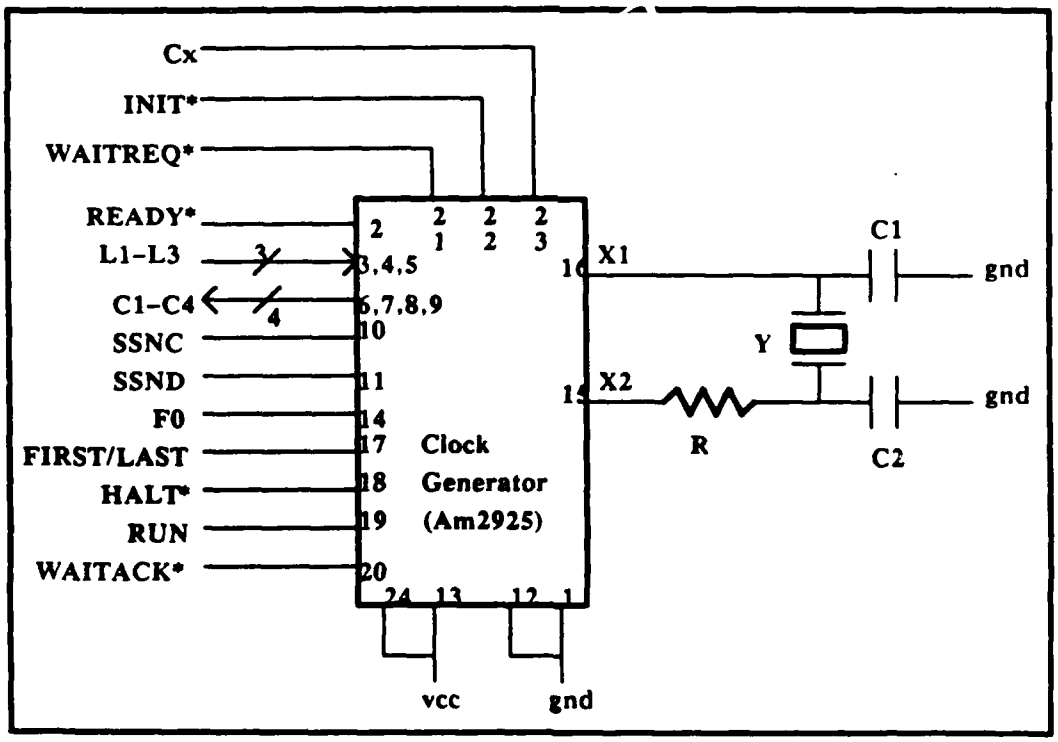


**Figure IV-8. Schematic diagram of clock generator.**

**Switching Characteristics.** The clock outputs C1, C2, C3, and C4 are available at the output 23 ns after receipt of crystal controlled oscillator inputs X1 and X2. It takes 20 ns to initialize during power up of system (2 : 5-233). The switching waveforms are drawn and explained in (2 : 5-235).

**Two Phase Clock.** To generate the non-overlapping two phase clock, either the outputs of the Am2925 clock generator can be used as programmable duty cycle clocks or a separate two phase clock generator chip can be used. An available two phase clock generator chip Intel 8224, generates a two phase clock up to 17 M Hz but the two phases have non uniform pulse width. If output waveforms of Am2925 are used, the maximum clock frequency which can be achieved is 4.25 M Hz.

The circuitry used to generate two phase clock is shown in Figure IV-9. C2 output waveform (L1-L3 = LLH) is passed through a negative edge triggered J-K flip flop to generate a select signal. The select signal is used by data selector (74LS154) to select C2 input signal as one of its clock outputs. The delay of J-K flip flop and data selector is 22 ns and 18 ns respectively. As shown in the timing analysis shown in Figure IV-9, the maximum clock frequency of each phase is 1/16th of the crystal frequency. Hence by using 30 M Hz crystal, 2.25 M Hz two phase clock can be generated.

### 4.8. Address Generator

The 31-bit address generator is designed to generate 31-bit sequential memory addresses as and when required by the user application. It is implemented with four SN74AS868 8-bit up/down counters, cascaded together to form a 31-bit counter. The counter receives initial input from

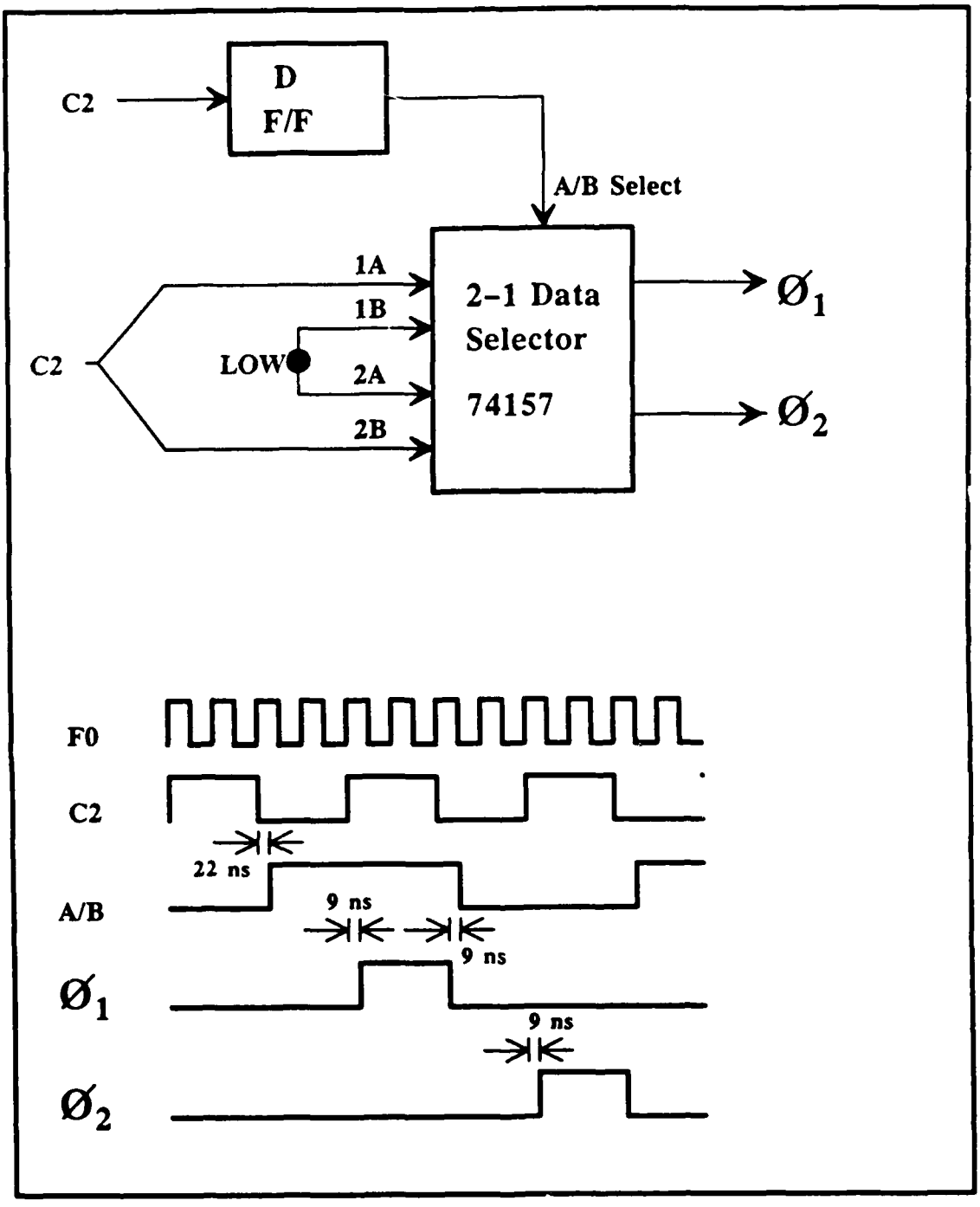


Figure IV-9. Schematic diagram of two phase clock generation.

the user application and its outputs are connected to AVDB address bus through a tristate isolator.

**Schematic Description.** The schematic diagram is drawn in Figure IV-10. The inputs of each U40 through U43 counters are connected to the user application. The buffers U44 through U47 are used to isolate the generated addresses from the AVDB address bus. The output enable signal is set HIGH to connect and LOW to disconnect.

**Modes of Operation.** The address generator has four modes of operation which can be selected by inputs S0 and S1. The contents of the address generator are cleared on low-to-high clock transition if both S0 and S1 are LOW. If both S0 and S1 inputs are HIGH, the addresses are generated upward and if S1 is LOW and S0 is HIGH, the addresses are generated downward. The inputs are loaded in to the address generator on clock pulse low-to-high transition if S1 is HIGH and S0 is LOW.

**Electrical Characteristics.** The set up time for S0 and S1 for load and clear mode is 13 ns and for count up and count down mode is 52 ns. The maximum permissible clock frequency is 6 M HZ which cannot be optimized because of four counters cascaded (each one can operate at up to 40 M HZ clock) (13 : 2-611).

### 4.9. Storage And Diagnostic Register

The 32-bit storage and diagnostic register is an high-speed parallel in/parallel out and serial in/serial out register which can be used either as a general purpose pipeline register or as a diagnostic register.

**General Description.** The register is implemented by using Am29818 which is a high-speed, general purpose pipeline register with an

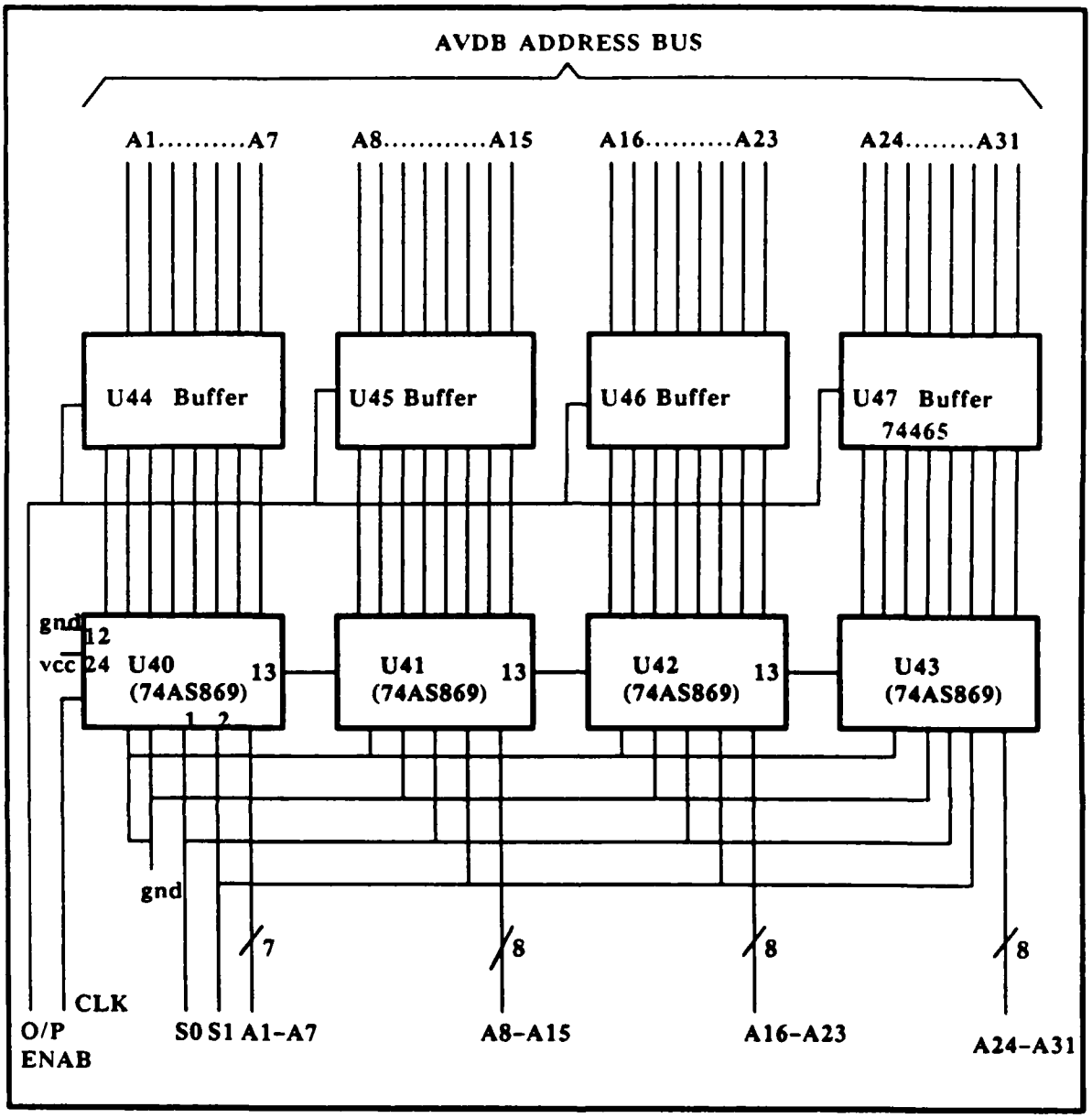


**Figure IV-10. Schematic diagram of address generator.**

on-board shadow register for performing diagnostics. The pipeline register receives data from data bus through the tristate buffers and its output can be extracted by user application. The data can be exchanged between pipeline register and shadow register by setting the appropriate inputs (2 : 8-15). The shadow register diagnostic capability provides the necessary functionality as well as a systematic method for detecting and pin-pointing hardware related failures in a system. It establishes a desired set of inputs, samples the necessary outputs, and determine whether the system is functioning correctly.

The shadow register diagnostics provides sufficient observability and controllability to turn any sequential network in to a combinational network. This is accomplished by providing the means to initialize and sample the state elements of a sequential network (2 : 8-16). In effect, the shadow register breaks the normal feedback path of the sequential network and establishes a logical path with which input can be defined and the output can be sampled. The techniques developed to test the combinational networks can be applied to any sequential network in which shadow register diagnostics has been utilized. There are two independent clock inputs (DCLK and PCLK). The input data can be shifted in shadow register via DCLK and loaded in to pipeline register via PCLK simultaneously.

**Schematic Description.** The schematic diagram of the storage and diagnostic register is drawn in Figure IV-11. Four Am29818 (U48 through U51) are cascaded to implement 32-bit storage register. The buffers (U52 through U55) are used to isolate it from AVDB data bus. The board data bus is connected by setting enable signal LOW. The SDI and SDO are the serial input and serial outputs of shadow register respectively. The OEY*,

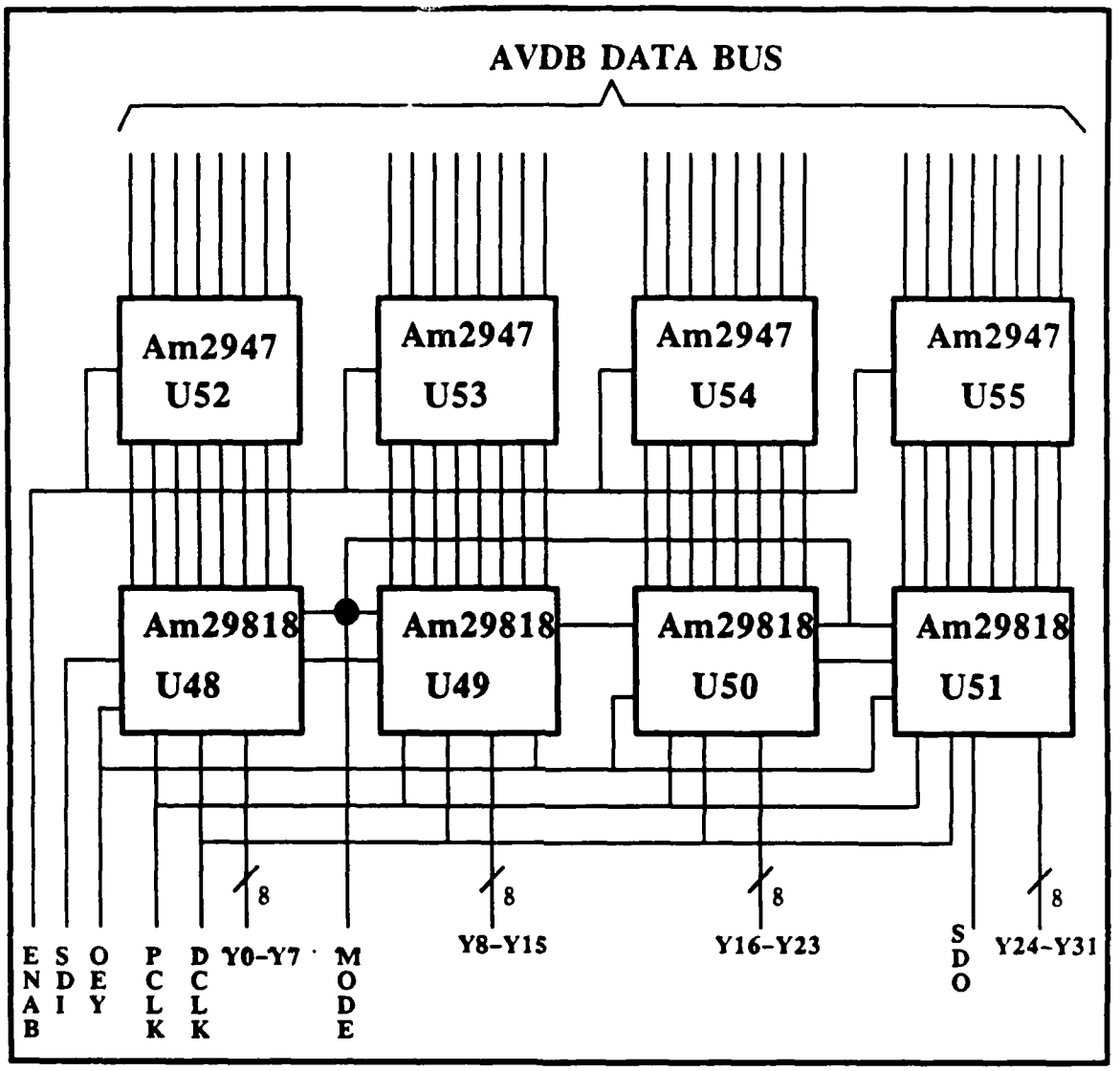


**Figure IV-11. Schematic diagram of diagnostic/storage register.**

if set LOW, put pipeline register output to the user application.

**Functional Description.** The four control inputs (SDI, MODE, DCLK, and PCLK) and the corresponding operations are given in Table IV-2. The data transfer in to the shadow register occurs on low-to-high transition of DCLK and MODE and SDI determine what data source will be loaded. The pipeline register is loaded on the low-to-high transition of PCLK and the MODE selects whether the data source is the data bus or the shadow register output (9:8-16).

**Switching Characteristics.** The maximum operable PCLK is 33 M HZ (15 ns HIGH and 15 ns LOW) and the maximum operable DCLK is 20 M HZ (25 ns HIGH and 25 ns LOW). All other parameters are described in detail in (2 : 8-20,21).

### 4.10. Bus Controller

The bus controller is implemented to control the usage of the AVDB data and address busses. There are six different devices connected to either data bus or address bus.

**Schematic Description.** The bus controller is implemented simply by using a 10-bit high performance bus interface register U56 (Am29821). The schematic diagram is drawn in Figure IV-12. The inputs from the user application are loaded in to the bus controller on low-to-high transition of load signal. The outputs can be enabled by setting OE* signal LOW. The control bit will be set to zero for the device being selected and the rest of the bits will be set HIGH by pull up resistors (U70). The typical propagation delay across the bus controller is 7.5 ns (2 : 8-23). The bus controller output bits and their respective devices are listed below.

Table IV-2. Modes of operation of storage/diagnostic register.

| Inputs | | | | operation |
|---|---|---|---|---|
| SDI | MODE | DCLK | PCLK | |
| X | L | ↑ | X | Serial shift shadow register |
| X | L | X | ↑ | Load pipeline register from data bus |
| L | H | ↑ | X | Load shadow reg. from user application |
| X | H | X | ↑ | Load pipeline register from shadow reg. |

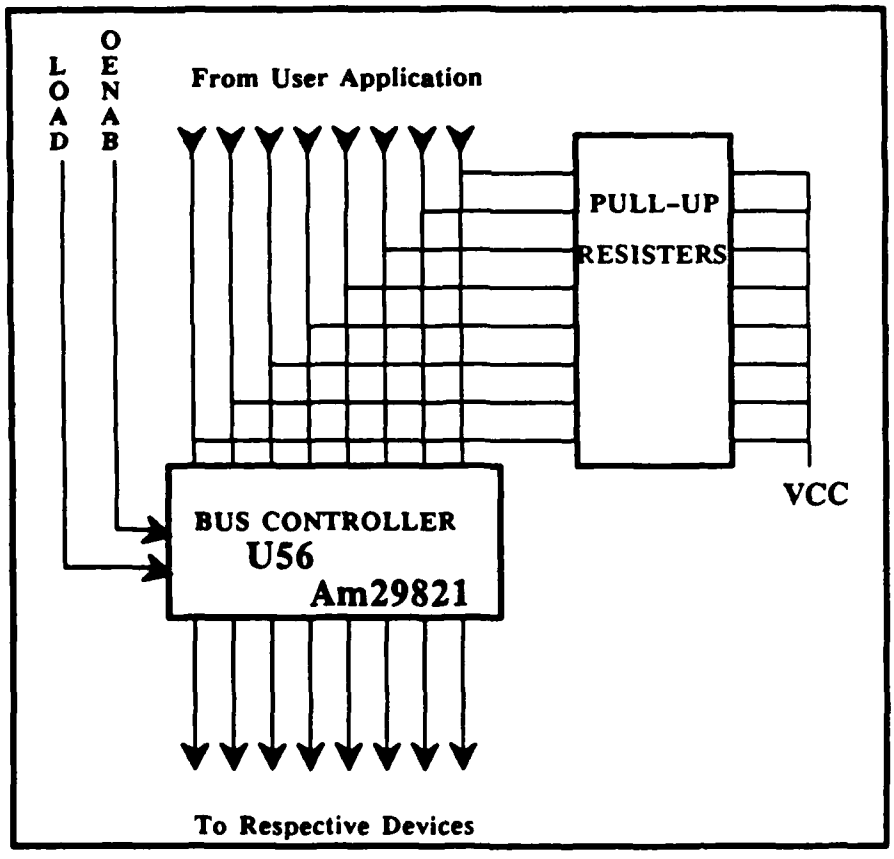


Figure IV-12. Schematic diagram of bus controller.

| Bit # | Device | Connected to |
|---|---|---|
| 0 | I/O | Data bus |
| 1 | I/O | Address bus |
| 2 | Storage register | Data bus |
| 3 | Address generator | Address bus |
| 4 | DMA controller | Address bus |
| 5 | DMA controller | Data bus |
| 6-9 | Not used | |

### 4.11. I/O Interface

The AVDB provides two parallel and two serial I/O ports for intercommunication between external devices.

### 4.12. Parallel I/O interface

There are two parallel I/O(PIO) ports provided for the user application. Each port is 8-bit wide and additional signals are also available for control and synchronization. The addresses 05H and 04H on eight least significant bits of address bus allow port A to interpret 8-bit data input as command and data respectively whereas the respective addresses for port B are 07H and 06H. The data transfer between user application and peripheral device is accomplished under interrupt control and the PIO can be programmed to interrupt the user application on the occurrence of specified status conditions in the peripheral device.

**Schematic Description.** The schematic diagram of both parallel and serial I/O interface is drawn in Figure IV-13. The parallel ports A and B are implemented by using single Z80 PIO (U57) which provides a TTL

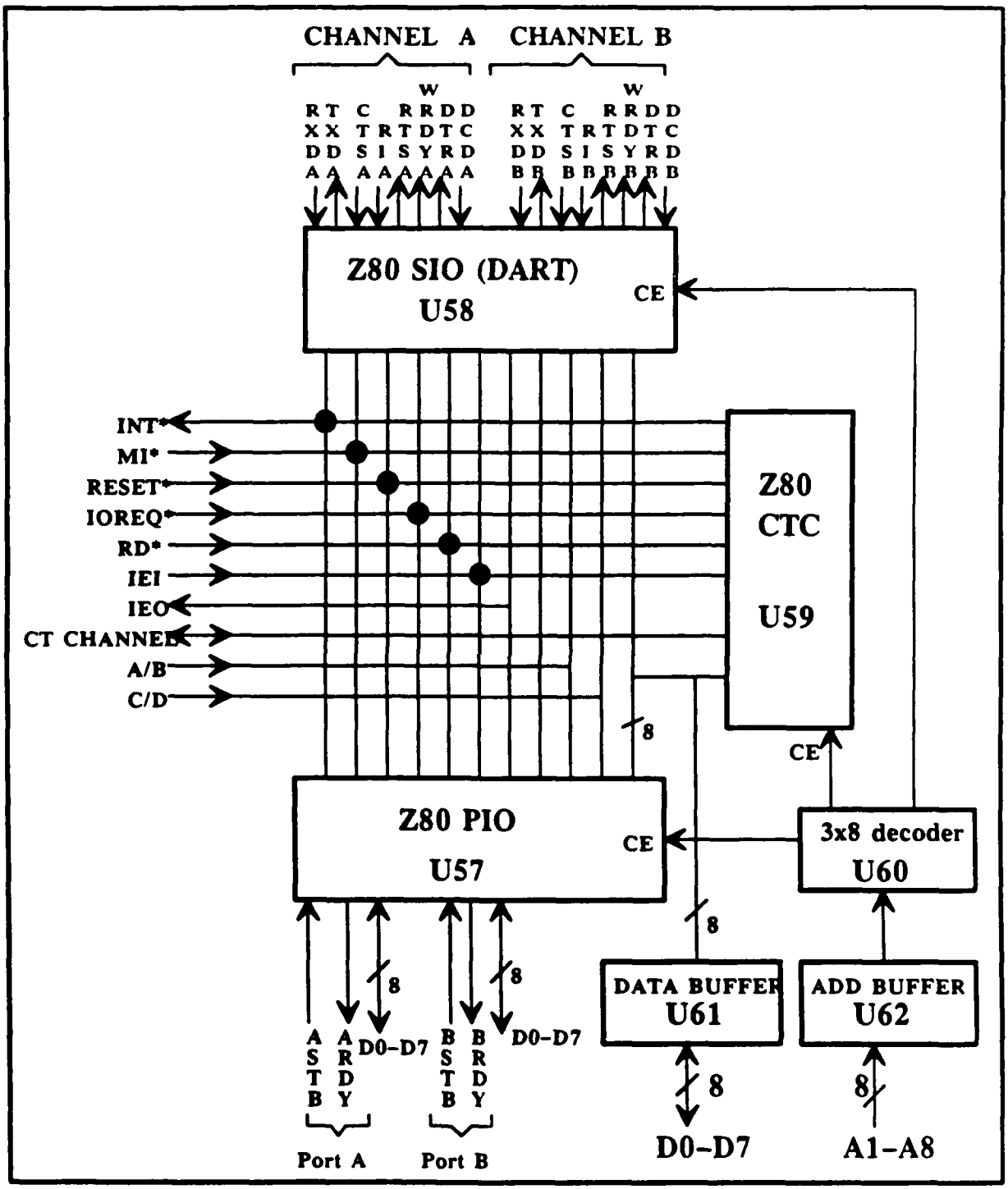


**Figure IV-13. Schematic diagram of serial/parallel I/O interface.**

compatible interface. The 3 to 8 bit decoder LS1386 (U60) is used to decode addresses for addressing the appropriate peripheral. The buffers U61 and U62 are used to isolate data and address lines. The U56 is a controller/ timer (Z80 CTC) which is used to generate I/O timings. The MI* signal is used as a sync pulse to control several internal PIO operations. When MI* is HIGH and RD* is HIGH, the application is fetching an instruction. Conversely, when MI* is HIGH and IOREQ* is HIGH, the application is acknowledging an interrupt. The IOREQ* signal is used in conjunction with the B/A select, C/D select, CE*, and RD* signal [14:5]. The RD* signal, if LOW, determines that I/O read operation is in progress. The IEI and IEO are the interrupt enable input and interrupt enable output signal respectively. The ASTB* and BSTB* are the acknowledging signals from the peripheral and the ARDY and BRDY are the readiness signals for port A and B respectively.

**Electrical Characteristics.** The timing associated with the output mode is illustrated in Figure IV-14a. A WR* pulse is generated by the PIO when RD*, CE*, C/D, and IOREQ* are active and is used to latch the data from the AVDB data bus in to the port's output register. The rising edge of the WR* pulse then raises the READY flag after the next falling edge of clock. The READY signal will remain active until a positive edge is received from the strobe line indicating that the peripheral has taken the data. The positive edge of the strobe pulse generates an interrupt request by setting the INT*(Interrupt input) LOW.

The timing associated with input cycle is illustrated in Figure IV-14b. The peripheral initiates this cycle using the strobe line. A LOW level on this line loads data in to the port input register and the rising edge of the

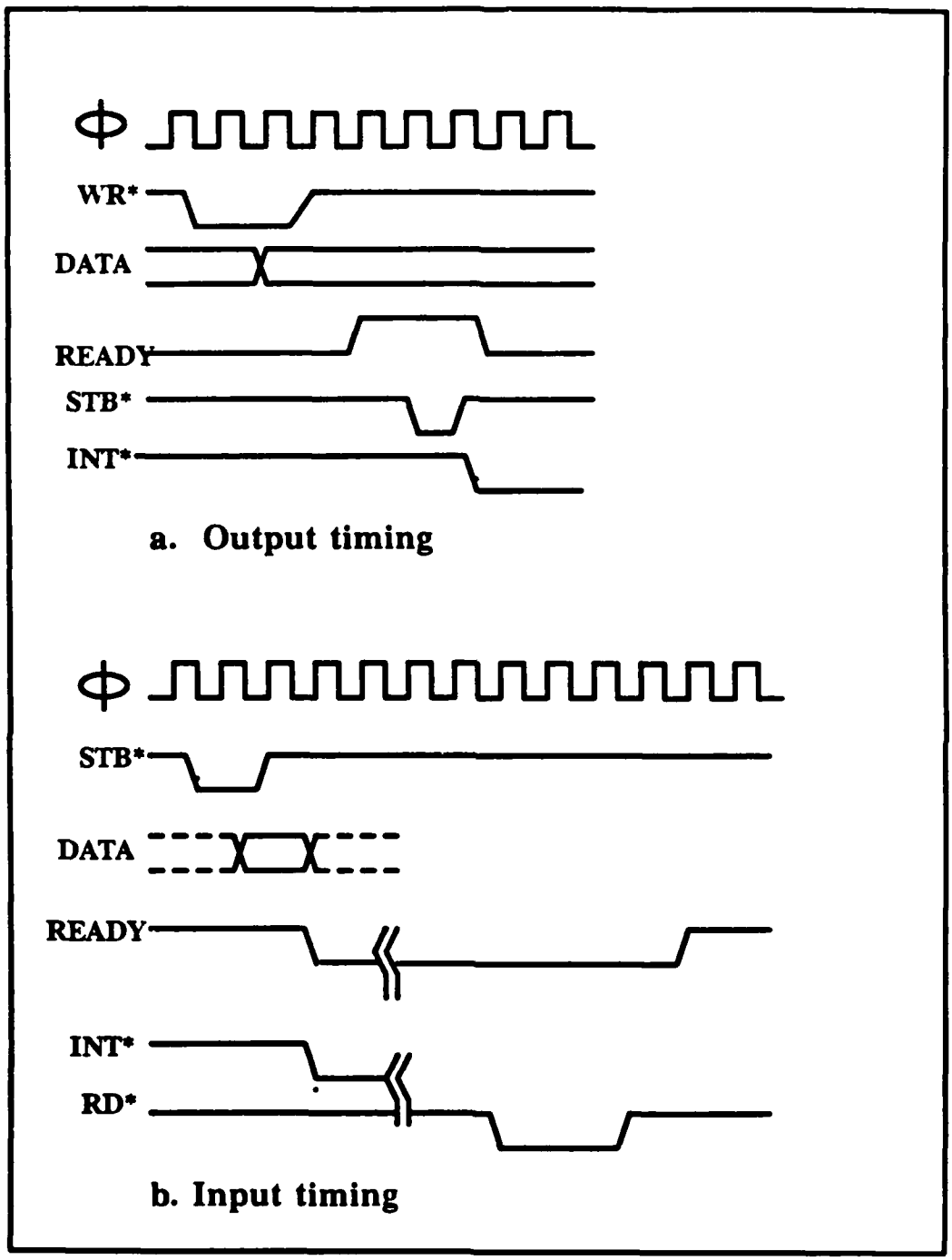


**Figure IV–14. Timing diagram of parallel I/O interface.**

strobe line activates the interrupt request line (INT*). The next falling clock edge will reset the READY line to active state to inhibit further loading. The user application then reads in the data from the interrupting port. When this occurs, the positive edge of RD* signal (initiated by user application) will raise the READY line on next falling edge of clock, indicating that new data can be loaded in to the PIO (15 :5).

### 4.13. Serial I/O Ports

The interface provides two independent full duplex channels (A,B). Their basic function is to control serial-to-parallel and parallel-to-serial conversion of the data inputs. The addresses 01H and 00H on eight least significant bits of address bus allow channel A to interpret 8-bit data input as command and data respectively, whereas the respective addresses for channel B are 03H and 02H.

**Schematic Description.** The schematic description of serial I/O interface is shown in Figure IV-13. The interface has been implemented by using Z80 SIO (U58) which is a dual channel multi-function peripheral component designed to satisfy a variety of serial data communication requirements. The common inputs for SIO and PIO are described earlier in PIO interface section. The CTSA* and CTSB* are the clear to send signals for respective channels and are issued by the peripheral during transmission. The DCDA* and DCDB* are data carrier detected inputs from peripheral activated during reception. The RXDA and RXDB are the receive data inputs from peripheral and TXDA and TXDB are the transmit data output from SIO. The RXCA and TXCA are the receiver and transmitter clock inputs respectively. The RTSA is a request to send signal selected by SIO and DTRA is the data terminal ready signal initiated by SIO. The

SYNCA* and SYNCB* are the synchronization inputs/outputs (13 : 2-4).

**Electrical Description.** The timing signals associated with read and write cycle are illustrated in Figure 15a and Figure 15b respectively. With 2.5 M HZ system clock rate the data can be transferred at 0-550 K bytes per second. The AC characteristics are described in (13 : 2-43).

### 4.14. VME Interface Chip

Single chip 32-bit DMA controllers and magnitude comparators are not available on the market and cascading bit slice components affect the efficiency, degrades the response time, and consumes excessive space on AVDB. Available 8 and 12 bit packages are required to implement a single selectable 31-bit comparator (Figure IV-1). If additional comparators are required to monitor different addresses simultaneously, the number of packages required is further multiplied. Similarly eight 8-bit DMA controller chips are required to implement one 32-bit DMA controller (Figure IV-4). Moreover the interrupt handler also consists of four packages (Figure IV-5).

The movement of data off-chip posses delays which are not acceptable for certain applications. To eliminate this problem, a VLSI VME interface chip (VIC) which interfaces to the VME bus has been designed (4:72) and is being implemented which interfaces the VME bus. The VIC functions as a 31-bit magnitude comparator, a DMA controller, and an interrupt handler.

The 31-bit comparator in the VIC is lazer programmable which allows each chip to be programmed with the desired address. The VIC chip at the most can support data transfers at 16 M bytes per second (4:77). This rate may decrease depending upon other system interrupts during transfer.

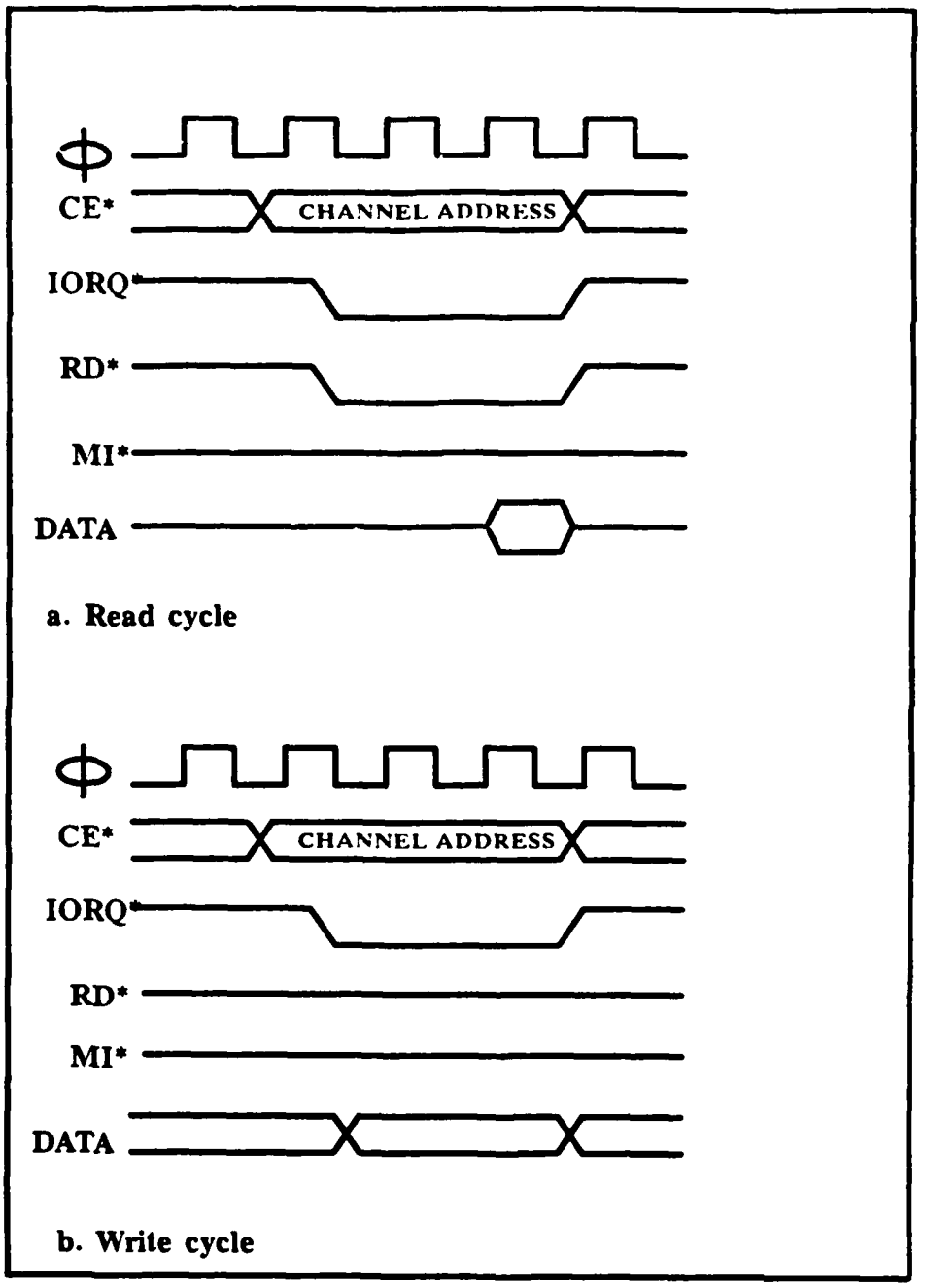


**Figure IV–15. Timing diagram of serial I/O interface.**

### 4.15. Bus Drivers

The appropriate line drivers are used on VME control lines depending upon the requirement of the AVDB functioning as Master or Slave. The Master/Slave pin of VIC chip controls the operation of these drivers as per VME specifications. As shown in Figure IV-16, 74LS245 transceivers (U105 and U106) are used to drive address modifier (AM0-AM5) signals, DTACK, WRITE, DS0 and DS1, IACK, and BERR signals. The 74S38 line driver (U107) is used to drive BBSY, IREQx, and BRx signals. The 74LS241 (U108) is used to drive the IACKOUT signal. All these drivers are suggested by and meet the VME specifications.

### 4.16. Schematic Drawing of AVDB

The schematic drawing of whole AVDB using VIC is drawn as Figure IV-16. The P1 and P2 are the VME bus 96-pin connecters and the remaining all the connectors are used to terminate the required signals in the user application area. The J1 and J5 are used for starting address of the address generator. The input and output data of the storage/diagnostic register is connected to J6 and J9. The J3 and J4 connecters are used to terminate the control signals for address generator and storage register respectively. The external I/O devices will be connected to either J10 and J11 (PIO) or J7 and J8 (SIO). The bus control and clock control signals are terminated at J13. The address bus is provided on J33 and J34 and the data bus is terminated at J31 and J32. The VIC control signals are terminated at J25 AND J26. The J22 and J24 are used to connect the bus grant in and out daisy chained signals and J21 and J23 are jumpers to select the appropriate interrupt request and bus request lines. The J30 is used for IACKIN and IACKOUT signal of the adjacent boards.

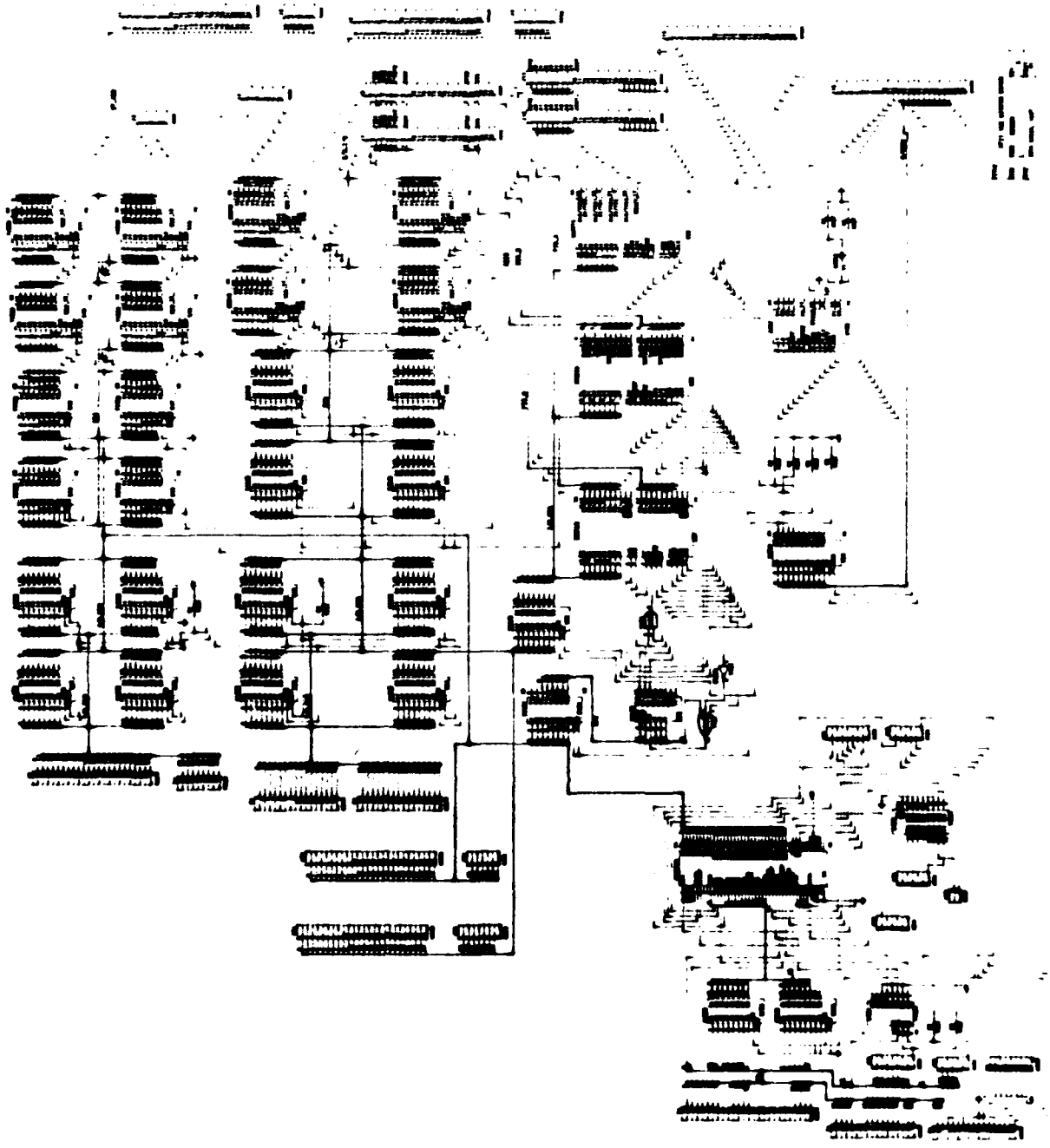

Figure IV-16. Schematic drawing of the AVDB.

# V. RESULTS AND ANALYSIS

The results achieved in this research are analyzed in this chapter. The circuitry discussed in the previous chapter is accommodated on the AFIT VME Design Board (AVDB) except the magnitude comparator, DMA controller, and interrupt handler which are replaced with VIC chip. Two PCB design tools were used to design the layout within the specifications of SUN workstations.

## 5.1. PCB Program

Prior to the procurement of DASH PCB design tool, a Printed Circuit Board (PCB) layout software was used to layout the components and to route the interconnecting wires between them. The PCB program was written to aid hardware design at Carnegie-Mellon University (CMU) and there was no commitment made to support this program for any other environments ( 1 ). The program supports four layers PCB design and graphic terminal interface is written for AED512 terminal. AFIT has a AED767 graphic terminal which is being used to support VLSI design projects. Efforts were made to change the AED interface portion of the PCB program, but the problem could not be resolved because of the software is not fully documented and the AED interface is distributed throughout the program. Hence, manual interaction could not be achieved. This proved to be a fatal flaw in the program because this PCB layout tool requires a graphic terminal.

The PCB program includes an automatic router which can be used without the graphic terminal. The automatic router was used to route the interconnecting wires but even with different placements of components, at the most 75 percent of the nets were routed by the PCB program. Without

the graphics interface working, the remaining nets cannot be realistically routed. The CIF plot as shown in Figure V-1 present the entire board layout with optimized placement of components that was obtainable.

### 5.2. PCB Program Overview

The PCB layout program is an integrated router and editor to design printed circuits. The components can be moved on a graphic screen and placed wherever desired to improve the routing. The automatic router routs the nets without the use of a graphic terminal and human intervention. The program also provides manual editing facilities where wires can be entered with a pointing device like a mouse. The wires can be erased either on individual basis or on entire area.

The PCB program generates a Caltech Intermediate File (CIF) which complies with the MOS Implementing Service (MOSIS) design rules for four layer boards. The internal database can be updated in order to add or remove nets and components. The net is a list of points which form an electrical connection and the component is a particular IC or any other actual device on a PC board.

There are three input files which describe the circuit, type file, component file, and netlist file. The type file contains the description and pin-locations of the used devices. The component file contains the names and types of all devices of the PC board. The component file can also contain the placement information i.e. where a particular device is located on the board. The netlist file describes all electrical connections that should be made.

**Drawbacks Rectified.** This research included the testing and evaluation of of the AFIT VME Design Board (AVDB) after getting it

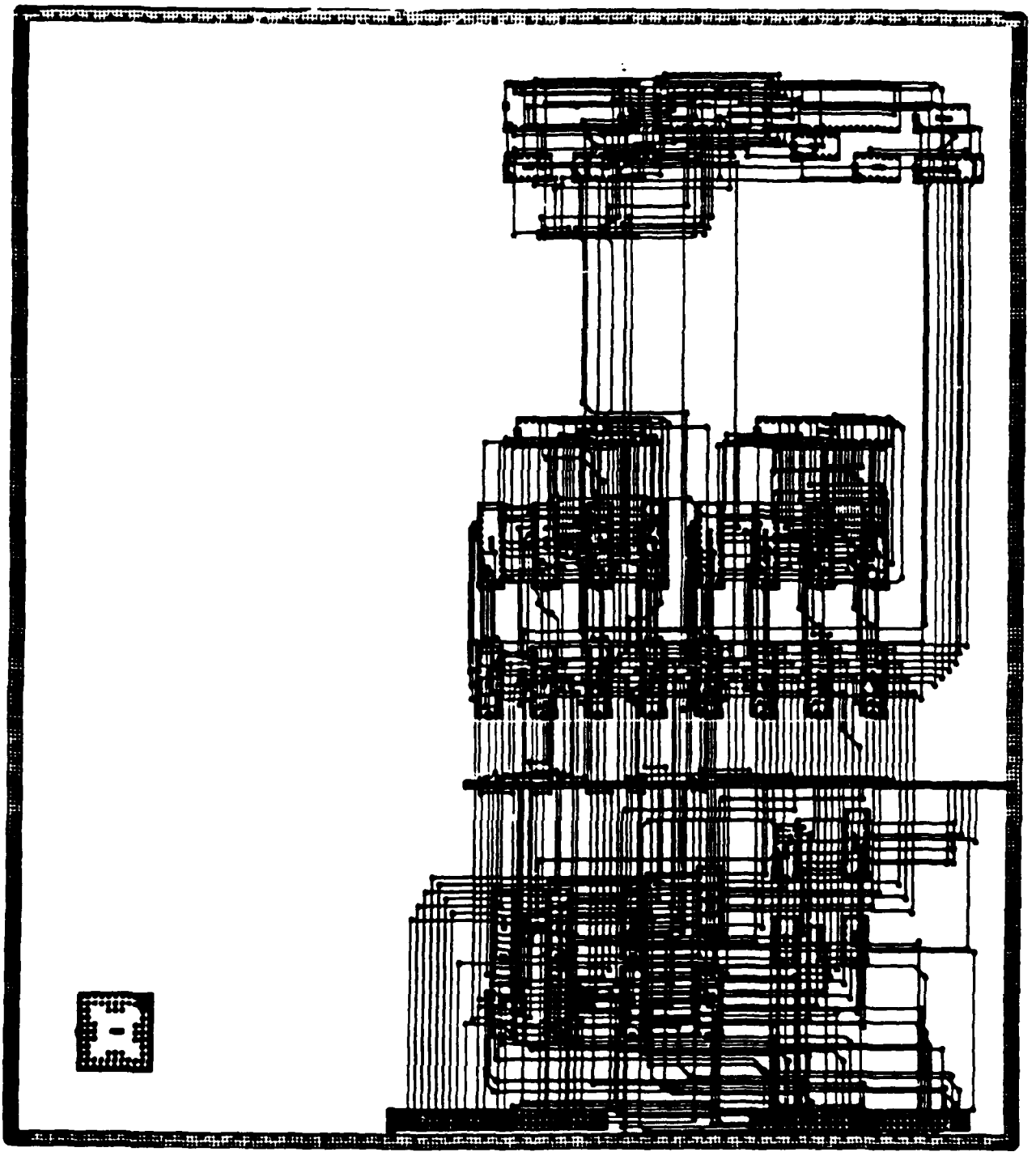

**Figure V-1. CIF plot of the AVDB with 75 percent routing.**

manufactured. But the bugs and shortcomings associated with the PCB program did not allow generation of a fully routed CIF file. The efforts were diverted to rectify the bugs in the PCB program and eliminate them. The following drawbacks were found and rectified.

**Board Size.** The PCB program did not accept board dimensions more than 30 Cm X 30 Cm whereas the AVDB size is 36.66 Cm X 40 Cm. The affecting variables, XMAX and YMAX, were found in pparm.h (program parameter definition) file. The values of these variables were increased and finally the program started accepting the required size of the board.

**AED File Reconfiguration.** The AED interface file of the program is reconfigured for AED767 terminal. The long hair cursor was changed to a regular small cursor which helped selecting different menus. The init() routine of paed.c file is sufficiently revised to work properly at AFIT which helped in eliminating undesired noise on AED terminal.

Maximum efforts were made to achieve optimum interface for AED767 but due to insufficient information available on PCB program, it could not be achieved. The originator ot the program also could not provide the solution to the problem. Only the lower left corner of the AVDB (12 Cm X 12 Cm) can be seen on the graphic terminal which is not sufficient for manual intervention. The Preview Window Size (PVWS) variable in pparm.h file was increased to increase the board area being displayed on AED terminal but no change was observed.

**Creation of CIF File.** The program did not produce a CIF file output in the beginning. On selection of CIF file output the program hung up without giving any error. The source codes of the relevant portions of the program were changed to increase the memory allocation for CIF file out-

put. The problem was corrected and a CIF file was produced from which CIF plots were generated. AS the size of CIF file increased, the fragmentation error started occurring which was eliminated by changing appropriate pointers in pcbsdef.h file.

**Outstanding Issues.** All the bugs in the PCB program could not be eliminated and following are the outstanding issues found and yet unresolved.

**Panning.** The panning facility helps to see desired portion of the PC board on the graphic terminal. The manual interaction to improve routing is done by panning through the board. The board outside the original display (12.5 Cm X 12.5 Cm) cannot be panned and seen on the screen. The original PROMS were also replaced in the AED767 terminal but did not help. This drawback was a setback factor for this research because the automatic router leaves some nets to be routed manually.

**AED Interface.** The AED interface file and the relevant portions in the entire PCB program needs to be found and rectified to reconfigure the codes from AED512 to AED767.

**Router Efficiency.** The program supports four layers including one power and one ground layer. With the available two signal layers the program is inefficient to completely route slightly congested PC boards. Due to shortage of signal layers an excessive number of VIAS are required to be made to change routes from layer to layer and thereby consume more space. For AVDB, the automatic router routed only 75 percent of the total nets on the board. The statistical data was collected for different placements of the components but 75 percent routing was the optimum and did not increase further. The PCB program needs to be modified for eight

layer board designs which will increase the routing efficiency.

### 5.3. DASH-PCB System

AFIT has recently acquired a new system for PCB designs which consists of DASH schematic editor, pinlist processor, DASH-PCB pinlist translator, and UNIX based PCB programs. The major features of the DASH-PCB system are listed in Table V-1 (12). The system is installed on IBM PC-AT and supports 10 layer PCB designs which overcomes the shortcoming of the existing 4 layer PCB layout software.

**Schematic Editor.** The schematic editor helps creating functional schematic drawings. The editor contains a schematic capture package, symbol libraries for most commonly used integrated circuits, and graphic editor which is used to create new symbols. For this research most of the packages were manually created using graphic editor. This is an interactive schematic editor that deals with four basic types of graphic items. The package symbols can be created and modified to represent the electronics components. The lines are drawn to show the interconnecting wires and busses. Alphanumeric fields are used to name the symbols. Different sizes of areas can be drawn, moved, and saved (11).

The system has its own symbol library of most commonly used components. However, the library can be updated and new symbols can be designed and inserted in the library database by using the graphics editor.

**Pinlist Processor.** The pinlist processor verifies the accuracy of schematic drawing and extracts a list of pins of all the packages. It also provides the signal description of the lines to which each pin connects.

Table V-1. Major features of DASH-PCB system.

| Feature | Description |
|---|---|
| Board Size | 32" X 32" maximum |
| Parts per Board | 200 unique parts maximum |
| Grid Size | 7 to 10 mils in 1 mil increment |
| Layers | maximum 10 layers with or without power and ground planes |
| Pins per package | 99 maximum |
| Pins per Network | 750 maximum |
| Router rule files | |
| Standard | Grid 25 mils<br>Trace width 12 mils<br>Space between traces 13 mils |
| Fine line | Grid 20 mils<br>Trace width 10 mils<br>Space between traces 10 mils |
| Package placement | Interactive |
| Display scale | 0.03 to 7.9 |
| Symbol libraries | TTL, Motorolla, CMOS, Intell, Memory |
| Router algorithms | Straight line, L-shape, Stairstep, maze, Custom |
| Board checking | Rules violation<br>Netlist verification |
| Postprocessing | penplots<br>Photoplots<br>Drill tape files<br>Parts list<br>Fabrication and assembly drawings |

**Pinlist Translator.** The pinlist translator program takes the pinlist. extracts data, and produces output files that become input for DASH-PCB programs. The files created are the parts library file (.PLB), the partslist file (.PRT), the schematic netlist file (.SNL), and the report file (.RPT). The first three files are input to DASH-PCB program and contain all the information it needs to create a PC board layout. The report file describes the packages used alongwith any unused or unplaced gates.

**DASH-PCB Programs.** The DASH-PCB programs run under PCBUNIX operating system. The system is supplied with standard and fine line rule files for 2 to 10 layer boards with optional separate power and ground planes. A rule file contains data that tells the router about the width of the traces, the minimum allowable space between traces, and the router grid size. For example the standard rule file allows 12 mils trace width, 25 mils grid size, and 13 mils minimum space between the traces. Whereas the fine line rule file allows 10 mils trace width, 20 mils grid size, and 10 mils minimum space between the traces. If required, a new rule file with desired parameters can be edited and used.

### 5.4. Results

The schematic diagram of AVDB is drawn and shown as Figure V-2. To ensure its accuracy a pinlist was obtained by using DASH pinlist processor. The pinlist translator was used to obtain the input files for DASH-PCB programs.

To achieve the AVDB layout, a job was setup 8 layers including two power and ground planes. The component side is the front layer and the solder side is the back layer. The internal layers from front to back in sequence are INT2, INT3, ground plane, power plane, INT4, and INT1.

The front, INT1, and INT3 signal layers contain the horizontal traces while the back, INT2, and INT4 signal layers contain the vertical traces.

The DASH EMS1 router was used to achieve automatic routing of the AVDB. The other available router EMS2 is a maze router which is used to improve the routing completion for only two layer boards. The AVDB design was initially started with four layers but the router could not route more than 40 percent of the total 659 traces. Then six layers were used to route the entire board but the routing completion was increased to only 60 percent. The unrouted traces were tried to be manually routed but the available space was not sufficient.

Finally, eight layers were used with separate power and ground planes. The six signal layers resulted in 90 percent routing completion which was improved to 94 percent by by optimizing the packages placement. By increasing the number of layers, the number of vias were also reduced. The router routed 625 traces out of 659 traces by making 553 vias. The remaining unrouted traces were manually routed by using graphic interaction. The time taken by the router increases for more congested boards and for AVDB it took 840 minutes to complete the routing.

The system allows the inclusion of keep-in-border to define the usable space for traces which helped getting about half of the board space unused for the user application. Figure V-2 presents traces and padsmaster of the front and back layer and Figure V-3 shows traces and padsmaster of INT1 and INT2. The traces and padsmaster of INT3 and INT4 are shown in Figure V-4. Finally Figure V-5 presents the ratsnest of the entire board which shows pin to pin straight line connections to determine the congested areas of the board. The ratsnest helps optimizing the placements for maximum

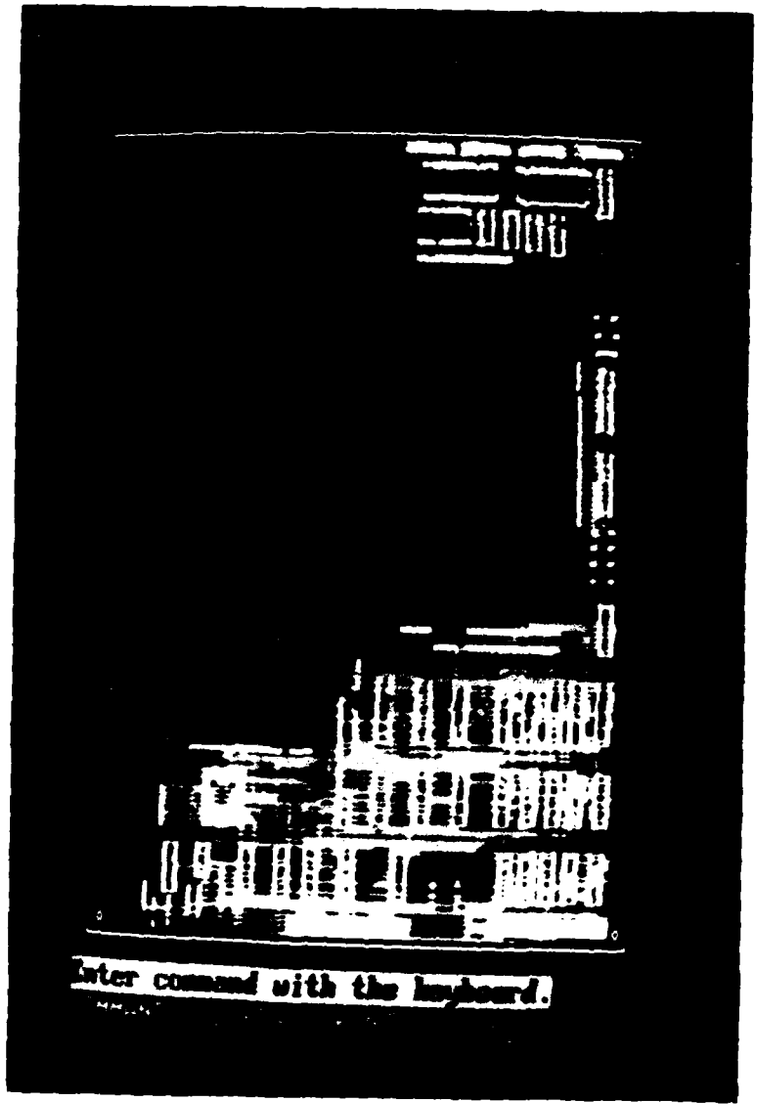


**Figure V–2. Traces and padsmaster of front and back layers.**

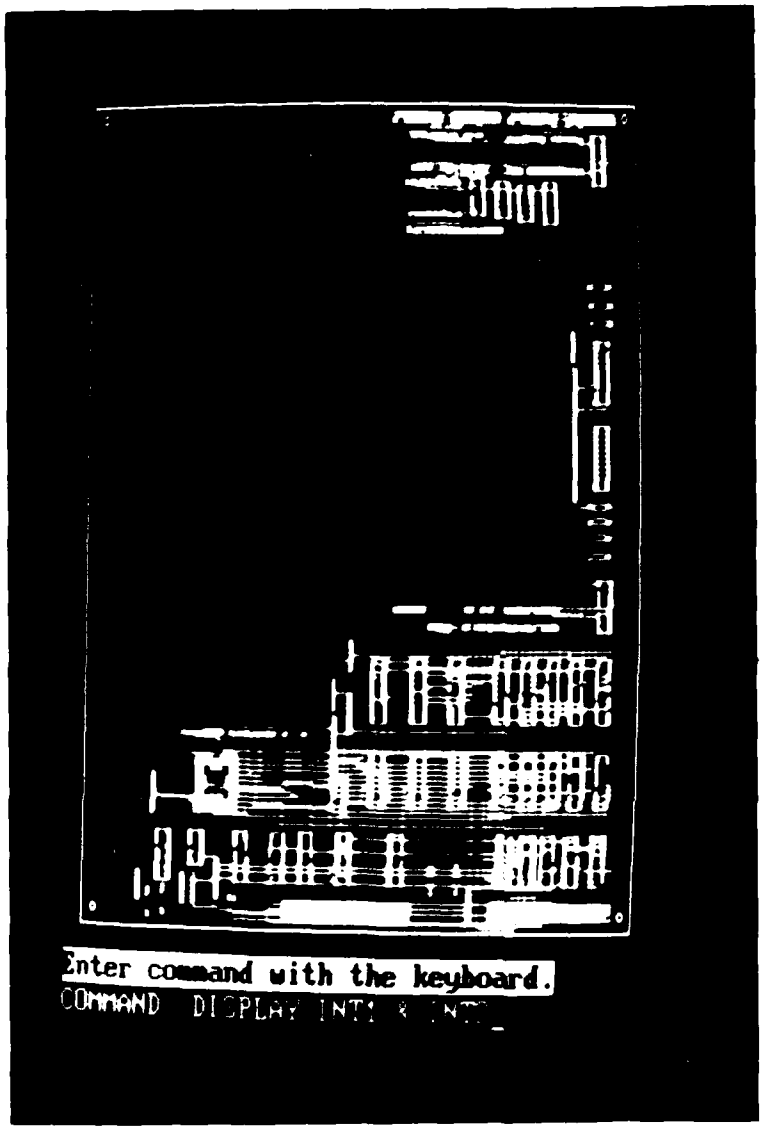


**Figure V-3. Traces and padsmaster of INT1 and INT2 layers.**

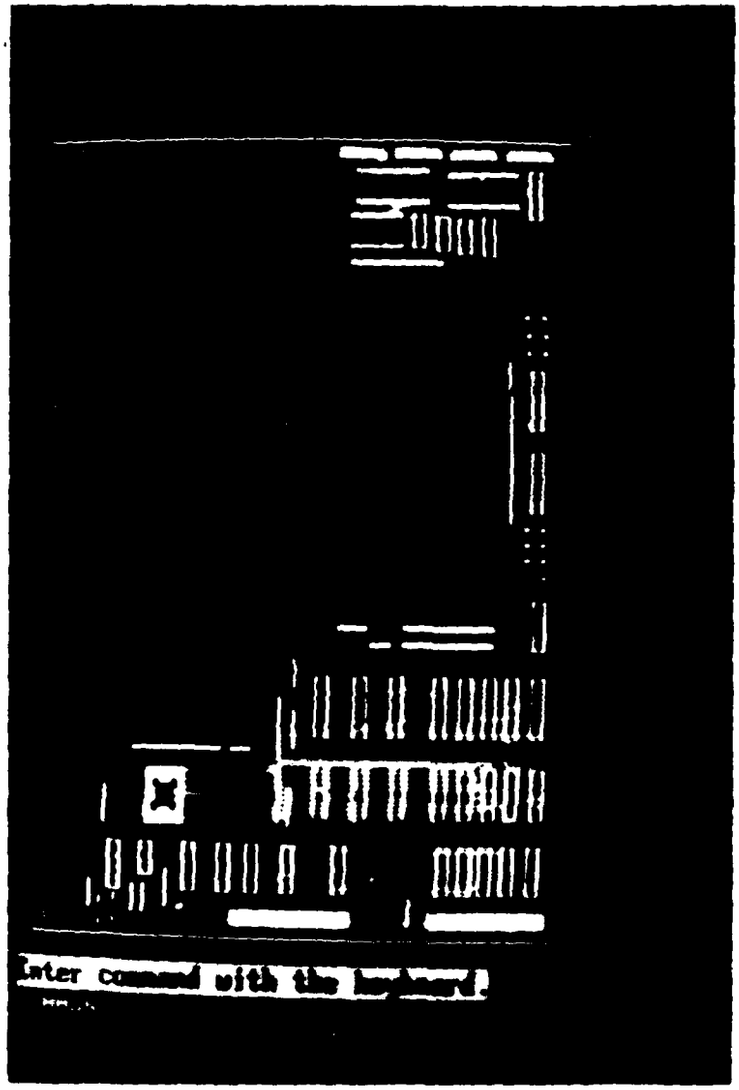

**Figure V–4. Traces and padsmaster of INT3 and INT4 layers.**

**Figure V-5. The ratsnest of the AVDB.**

routing results.

The HP plotter 7580B was used to plot these Figures which drew some undesired lines which are actually not present on the board. The undesired lines are probably generated due to improper interface between the IBM PC and the plotter. Asci files have been obtained which can be used to generate photoplots of each layer.

# VI. CONCLUSIONS AND RECOMMENDATIONS

## 6.1. Conclusions

A detailed approach for a design of a general purpose printed circuit board has been defined and specified. The purpose of this research is to provide a general purpose VME based multilayer board frame which can be used for a variety of applications.

The most commonly used facilities like a bus interface, testing support, and an interface for external Input/Output devices are specified and circuitry is designed to implement each of these requirements. The two available PCB layout software were used to layout the AVDB and route the interconnecting wires between the onboard chip packages. Due to the limitation on maximum number of layer of board designs supported by the software and an inadequate interface for the available graphic terminal, the complete routing could not be achieved on PCB layout system.

The Futurenet schematic designer DASH-4 (made available at the end of this research) was used to draw the schematic drawing of the complete AVDB. An error free schematic drawing was used to obtain the pinlist of all the components. The pinlist translator was used to generate the required input files for DASH-PCB program. The packages were placed at optimized places and the automatic router was used to obtain the routing of interconnecting traces. The traces were routed using fine line rule file which allows 20 mils grid size, 10 mils trace width, and 10 mils minimum space between the traces.

The postprocessing program was used to obtain penplots of all the signal layers of the AVDB. All the requirement of PCB manufacturer have been met and the AVDB is ready for submission to any appropriate

organization for manufacturing. The AVDB however, can not be manufactured through MOSIS because a CIF file is not one of the output of BASH-PCB system. The DASH output files may be converted to MOSIS compatible CIF file if AVDB is required to be manufactured through MOSIS.

### 6.2. Recommendations

It is strongly recommended that this research may be continued and final product (AVDB) be manufactured. The AVDB then needs to be tested on bench as well as inside the system (SUN Workstation). A specific application like CAM system may then be added to the board for system evaluation.

For the CAM system, the user application area can hold 16 CAM chips, RISC chip, and other associated circuitry. However if more memory space is required to be established, separate daughter boards can be used. Each daughter board can hold 121 84-pin CAM packages.

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## VITA

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Block 19 Continued:

This thesis investigates the design of an AFIT VME design board. This effort concentrated on implementating a prototype general purpose printed circuit board for SUN/3 Workstation. This thesis presents detailed design of the functional blocks like VME interface, testing electronics, and Input/Output interface. The board size is 14.5" x 15.125" and about half of the board is left unused for user application. The user can implement a specific circuitry in the provided space for testing in a real time environments.

An eight layer printed circuit board has been layed out and routed using DASH-PCS design system. The final product will be a valuable tool for testing VLSI chips and other applications in a real time environments.

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